RECEIVED
CENTRAL FAX CENTER

APR 1 1 2007

PATENT
P54757RE2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Application of: OK-HYUN SON

Appeal № _____

Original Patent № 5,963,387 issued on 5 October 1999

Serial No.:	09/971,081	Examiner:	HABERMEHL, JAMES LEE
Filed:	5th of October 2001	Art Unit:	2627

For: METHOD FOR FORMING AND PROCESSING DATA ADDRESS MARK FOR HARD DISK DRIVE

APPEAL BRIEF

Paper № 29

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313.1450

Sir:

In response to the Notification of Non-Compliant Appeal Brief (37 C.F.R. §41.37) mailed 11 January 2007 (Paper No. 20070109), and pursuant to Appellant's Notice of Appeal filed on the 4th of October 2006, Appellant hereby appeals to the Board of Patent Appeals and Interferences from the final rejection of claims 1 through 54 as set forth in the final Office action mailed on the 4th of April 2006 (Paper № 20060328) and Advisory Action mailed on the 22nd of November 2006 (Paper № 20061120).

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that, on 11 April 2007, this correspondence is being facsimile transmitted to the U.S. Patent & Trademark Office (**Facsimile No. 571-273-8300**)

Total –112-- sheets

For Robert E. Bushnell
Reg. No. 27,774

Folio: P54757RE2
Date: 4/11/07
I.D.: REB/kf

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

Pursuant to 37 CFR §41.37(c)(1)(as amended), the real party in interest is:

Samsung Electronics Co., Ltd.

#416, Maetan-dong, Yeongtong-gu

Suwon-si, Gyeonggi-do, Republic of KOREA

as evidenced by the ***Assignment*** recorded by the U.S. Patent and Trademark Office on the 30th day of September 1997 at Reel 8757, Frame 0915.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals and no interferences known to Appellant, Appellant's legal representatives or the assignee which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1 through 54 are pending in the application, of which claims 1, 7, 11, 16, 20, 24, 26, 31, 32, and 35 through 54 are independent claims whereas the remaining claims are dependent claims. Claims 1 through 15 are original claims. Claims 3, 4, 7, 9, 16, 20, 23, 28, 31, 32 and 43 have been previously amended.

IV. STATUS OF AMENDMENTS

An Amendment After Final was submitted to the U.S. Patent and Trademark Office on the 4th of October 2006 requesting amendments to the specification. No claim amendments were proposed after issuance of the final Office action mailed on the 4th of April 2006 (Paper № 20060328). The Amendment After Final was not entered for the reasons stated in the 22nd of November 2006 Advisory Action (Paper № 20061120).

V. SUMMARY OF CLAIMED SUBJECT MATTER

Figure 1 illustrates a general track sector format of a magnetic disk using constant density recording.[1] The track sector format includes two successive data sectors between servo sectors of a magnetic disk [2] with each data sector subdivided into an identification (ID) field and a data field. Header information for identifying a corresponding data sector is written into the ID field. Actual digital data is written into the data field preceded by the ID field.

ID field consists of an ID preamble, an ID address mark, an ID, a cyclic redundancy code (CRC) and an ID postamble, as shown in Figure 2.[3] The ID preamble provides clock synchronization for the ID field during reading and simultaneously provides a gap before the ID field. The ID address mark informs that the ID is started and provides synchronization for reading the ID. The ID is the header information for identifying the sector in which a head is currently positioned, such as a sector number, a head number, a cylinder number, etc. The CRC is an error detecting code for detecting an error of the ID address mark and the ID. Generally, the CRC is generated by using a CRC-CCITT generating polynomial. The ID postamble provides a necessary timing margin after reading the ID.

---

1 Beginning in column 4, with line 3.

2 Claim 1, lines 1-2; claim 7, lines 1-2; claim 16, lines 1-2; claim 24, lines 1-2; claim 31, line 1; claim 38, line 1; claim 40, line 1; claim 41, lines 1-2; claim 42, lines 1-2; claim 43, lines 1-2; claim 47, line 1; claim 48, line 1; and claim 49, line 1.

3 Claim 8, lines 1-3; claim 15, lines 1-3.

A data field consists of a data preamble, a data address mark,[4] data,[5] a CRC and a data postamble, as shown in Figure 3.[6] Meanwhile, the data field of the magnetic disk using a headerless servo recording system is formed as shown in Figure 4. The data preamble positioned between the ID postamble and a data synchronizing bit provides clock synchronization for the data field during reading and simultaneously provides a gap between the ID field and the data field. The data address mark informs that the data is started and provides necessary synchronization when the magnetic disk driving apparatus reads the data.[7] The data is the actual digital information stored in the magnetic disk.[8] An error correcting code (EEC) is an error detecting code for detecting and correcting an error of the data. The data postamble provides a necessary timing margin after reading the data. Generally, since the ID post amble is adjacent to the data preamble, and the data postamble is adjacent to the ID preamble, they are mixedly used.

In contemporary disk drives using the foregoing recording format, if there is occurrence of a defect in a data area, damaged data can be restored by using the ECC. If there is occurrence of a defect in the data address mark area however, it is difficult, and probably not possible to

---

4 Claim 2, line 1.

5 Claim 1, line 7.

6 Beginning in column 4, with line 3 of Applicant's patent.

7 Claim 1, lines 2 and 7; claim 31, line 2; claim 47, line 2; claim 48, line 2; and claim 49, line 2.

8 Claim 1, lines 1-2 and 7; claim 31, lines 1-4; claim 47, lines 2-3; claim 48, lines 2-3; claim 49, lines 2-3; claim 50, lines 5-6; claim 51, lines 4-5; claim 52, lines 5-6.

restore the damaged data address mark. As a result, since the data address mark is not detected, data positioned at the data area following the data address mark can not be normally accessed. Moreover, if the data field is over its tolerance limits, the disk drive must be repaired or discarded, with a concomitant loss of valuable time and economy.

Figure 5 illustrates a high density hard disk drive HDD constructed according to the principles of the present invention is illustrated. The HDD includes, for example, two magnetic disks 2 [9] and corresponding four transducer heads 4, a transducer head assembly 6 in an E-shape having actuator arms 5 each for supporting a respective pair of transducer heads 4, a preamplifier 8, a read/write channel circuit 10, an analog-to-digital (A/D) converter 12, a track information detector 13, a micro-controller 14, a digital-to-analog (D/C) converter 16, a voice coil motor (VCM) driver 18, a voice coil motor 20, a motor controller 22, a spindle motor driver 24, a spindle motor 26 for rotating magnetic head 4 across the surface of disk 2, and a disk data controller (DDC) 28.

Preamplifier 8 is electrically connected to transducer head assembly 6 for amplifying a predetermined signal read from disk 2 using transducer head 4 [10] and transmitting the amplified

---

[9] Claim 5, lines 1-2; claim 6, lines 1-3; claim 11, lines 2-6; claim 16, lines 1-2; claim 20, lines 1-2; claim 24, lines 1-2; claim 26, lines 1-2; claim 31, line1; claim 35, lines 1-2; claim 36, lines 1-2; claim 37, lines 1-2; claim 38, line 1; claim 39, lines 1-2; claim 40, lines 1-2; claim 41, lines 1-2; claim 42, lines 1-2; claim 43, lines 1-2; claim 44, line 1-2; claim 45, lines 1-2; claim 46, lines 1-2; claim 47, line 1; claim 48, line 1; claim 49, line 1; claim 50, lines 1-2; claim 51, line 1-2; claim 52, lines 1-2; claim 53, line 1; and claim 54, line 1.

[10] Claim 25, lines 2-3; claim 26, lines 2-3; claim 24, lines 5-6; claim 32, lines 2-4; claim 33, line 2; claim 34, lines 2-3; 41, lines 6-7; claim 42, lines 6-7; claim 43, lines 6-7; claim 44, lines 2-4; claim 45, lines 2-4; 46, lines 1-2; claim 50, line 2; claim 51, line 2; and claim 52, line 2.

signal to the read/write channel circuit 10.[11] For the purpose of writing data onto disk 2,[12] preamplifier 8 applies encoded writing data transmitted from read/write channel circuit 10 to a designated transducer head from magnetic heads 4 to be recorded on disks 2.[13] At this time, preamplifier 12 selects one of magnetic heads 4 according to a control signal generated from a disk data controller (DDC) 28 under the instruction of a micro-controller 14.[14]

Read/write channel circuit 10 is connected between preamplifier 8 and DDC 28 for decoding data pulses from an input signal received from preamplifier 8 to generate read-out data RDATA, and for decoding writing data WDATA received from DDC 28 to transmit the decoded WDATA to preamplifier 8. Read/write channel circuit 10 generates a phase error signal (PES) by decoding head position information, *i.e.*, a part of servo information, which is recorded on the disk. The PES is then transmitted to micro-controller 14 via A/D converter 12. At this stage, A/D converter 12 converts the PES into a digital value corresponding to a predetermined

---

11 Beginning in column 5, with line 4.

12 Claim 1, lines 4-5; claim 7, lines 4-5; claim 11, lines16-17; claim 16, lines 1-5; claim 24, lines 5-6; claim 31, lines 2-6; claim 32, lines 5-6; claim 35, lines 3-5; claim 36, lines 3-5; claim 37, lines 3-5; claim 41, lines 2-5; claim 42, lines 6-7; claim 43, lines 6-7; 47, lines 1-2; claim 48, lines 1-2; claims 49, lines 1-2; claim 53, lines 3-4; and claim 54, lines 3-4.

13 Claim 1, lines 4-5; claim 2, line 1; claim 3, line 2; claim 7, lines 4-5; claim 11, lines16-17; claim 16, lines 1-5; claim 24, lines 5-6; claim 31, lines 2-6; claim 32, lines 5-6; claim 35, lines 3-5; claim 36, lines 3-5; claim 37, lines 3-5; claim 41, lines 2-5; claim 42, lines 6-7; claim 43, lines 6-7; 47, lines 1-2; claim 48, lines 1-2; claims 49, lines 1-2; claim 53, lines 3-4; and claim 54, lines 3-4.

14 Claim 11, lines16-17; claim 24, lines 5-6; claim 31, lines 2-6; claim 32, lines 2-6; claim 34, lines 2-4; claim 35, lines 3-5; claim 36, lines 3-5; claim 37, lines 3-5; claim 41, lines 2-5; claim 42, lines 6-7; claim 43, lines 6-7; 47, lines 1-2; claim 48, lines 1-2; claims 49, lines 1-2; claim 50, lines 2-6; claim 51, lines 2-5; and claim 52, lines 1-6.

level and transmits the converted PES to micro-controller 14.

Track information detector 13 is connected between read/write channel circuit 10 and micro-controller 14 for detecting from the RDATA, a track number for the current position of transducer head 4 and providing the detected data to micro-controller 14. DDC 28 is controlled by micro-controller 14 to record the data received from a host computer via read/write channel circuit 10 and preamplifier 8 or to transmit the data read out from disks 2 to the host computer.[15]

Micro-controller 14 controls DDC 28 according to a command received from the host computer to search a track and position of the transducer head.[16] In conducting a search and positioning the transducer head, micro-controller 14 uses the track number and the PES input from track information detector 13 and A/D converter 12, respectively. D/A converter 16 is connected to micro-controller 14 for converting the digital signal output from micro-controller 14 into an analog signal for controlling the position of transducer heads 4. VCM driver 18 generates a driving current for driving VCM 20 according to the analog signal input from D/A

---

15 Claim 1, lines 4-5; claim 7, lines 4-5; claim 11, line 7; claim 16, lines 1-5; claim 24, lines 5-6; claim 28, lines 3-4; claim 26, line 2; claim 31, lines 2-6; claim 32, lines 5-6; claim 35, lines 3-5; claim 36, lines 3-5; claim 37, lines 3-5; claim 38, lines 3-6; claim 39, lines 3-6; claim 40, lines 3-6; claim 41, lines 2-5; claim 42, lines 2-5; claim 43, lines 2-4; claim 44, line 2; claim 45, line 2; claim 46, line 2; claim 47, lines 1-2; claim 48, lines 1-2; claims 49, lines 1-2; claim 50, lines 2-4; claim 51, lines 2-3; claim 52, line 2-3; claim 53, lines 3-4; and claim 54, lines 3-4.

16 Claim 1, lines 4-5; claim 2, line 1; claim 3, line 2; claim 7, lines 4-5; claim 11, lines16-17; claim 16, lines 1-5; claim 24, lines 5-6; claim 31, lines 2-6; claim 32, lines 5-6; claim 35, lines 3-5; claim 36, lines 3-5; claim 37, lines 3-5; claim 41, lines 2-5; claim 42, lines 6-7; claim 43, lines 6-7; 47, lines 1-2; claim 48, lines 1-2; claims 49, lines 1-2; claim 53, lines 3-4; and claim 54, lines 3-4.

converter 16. VCM 20 drives transducer heads 4 to move in a radial direction of disk 2 corresponding to the level of the driving current input from VCM driver 18.

Motor controller 22 is connected to micro-controller 14 for controlling a spindle motor driver 24 according to a disk rotation control command output from micro-controller 14. Spindle motor driver 24 drives spindle motor 26 in accordance with the control of motor controller 22 to thereby rotate disk 2.

Figure 6 illustrates a detailed format of a data field constructed according to the principles of the present invention. Data address marks are constructed by two (2) bytes.[17] During the write operation of each sector, both first and second data address marks are written,[18] and the write operation is not concerned in the generation of an ECC.

The two data address marks are respectively distinguished by using different patterns,[19]

---

[17] Claim 1, lines 4-5; claim 7, lines 4-5; claim 11, lines16-17; claim 16, lines 1-5; claim 24, lines 5-6; claim 31, lines 2-6; claim 32, lines 5-6; claim 35, lines 3-5; claim 36, lines 3-5; claim 37, lines 3-5; claim 41, lines 2-5; claim 42, lines 6-7; claim 43, lines 6-7; 47, lines 1-2; claim 48, lines 1-2; claims 49, lines 1-2; claim 53, lines 3-4; and claim 54, lines 3-4.

[18] Claim 1, lines 4-5; claim 2, lines 2-5; claim 7, lines 4-5; claim 8, lines 2-4; claim 11, lines 6-7; claim 12, line 2; claim 12, lines 2-5; claim 13, lines 1-2; claim 14, lines 1-2; claim 16, lines 1-5; claim 17, lines 3-6; claim 21, lines 2-4; claim 24, lines 5-6; claim 28, lines 3-4; claim 26, line 2; claim 28, lines 3-7; claim 31, lines 2-6; claim 32, lines 5-6; claim 35, lines 3-5; claim 36, lines 3-5; claim 37, lines 3-5; claim 38, lines 3-6; claim 39, lines 3-6; claim 40, lines 3-6; claim 41, lines 2-5; claim 42, lines 2-5; claim 43, lines 2-4; claim 44, line 2; claim 45, line 2; claim 46, line 2; claim 47, lines 1-2; claim 48, lines 1-2; claims 49, lines 1-2; claim 50, lines 2-4; claim 51, lines 2-3; claim 52, line 2-3; claim 53, lines 3-5; and claim 54, lines 3-4.

[19] Claim 1, lines 4-5; claim 7, lines 4-5; claim 11, line 7; claim 16, lines 1-5; claim 24, lines 5-6; claim 28, lines 3-4; claim 26, line 2; claim 31, lines 2-6; claim 32, lines 5-6; claim 35, lines 3-5; claim 36, lines 3-5; claim 37, lines 3-5; claim 38, lines 3-6; claim 39, lines 3-6; claim 40, lines 3-6; claim 41, lines 2-5; claim 42, lines 2-5; claim 43,

and are distinguished by micro-controller 14. For example, the first data address mark is defined as "A1" and the second data address mark is defined as "A2".[20] The seven (7) most significant bits select any pattern defined as a user pattern and the least significant bit is used for counting the data address mark constructed by two (2) bytes.[21] During the read operation of each sector, when only one byte of data address mark is detected among two (2) bytes of data address marks, it is regarded as an effective data address mark. That is, if the first data address mark is normally detected, the second data address mark of one byte is skipped and the following information is regarded as data.[22] If the first address mark has a defect, however, the second data address mark is detected. If it is determined that the second data address mark is normally detected, the following information is regarded as data. Whether the read data address mark is the first data address mark or the second data address mark is determined by the recording patterns as previously determined during the write operation.[23] Meanwhile,

---

lines 2-4; claim 44, line 2; claim 45, line 2; claim 46, line 2; claim 47, lines 1-2; claim 48, lines 1-2; claims 49, lines 1-2; claim 50, lines 2-4; claim 51, lines 2-3; claim 52, line 2-3; claim 53, lines 3-4; and claim 54, lines 3-4.

20 Beginning on column 6, with line 1, and hereafter continuing on column 6, through line 53.

21 Claim 4, lines 2-4; claim 18, lines 2-3; claim 19, lines 2-3; claim 22, lines 2-3; claim 23, lines 2-3; claim 25, lines 2-4; claim 29, lines 2-4; claim 30, lines 2-3; claim 33, lines 2-4; and claim 34, lines 3-4.

22 Claim 1, lines 10-12; claim 7, lines 13-15; claim 11, lines 18-20; claim 12, lines 5-7; claim 13, lines 5-7; claim 18, lines 2-3; claim 19, lines 2-3; claim 22, lines 2-3; claim 23, lines 2-3; claim 25, lines 2-4; claim 27, lines 1-2; claim 29, lines 2-4; claim 30, lines 2-3; claim 33, lines 2-4; and claim 34, lines 2-4.

23 Claim 1, lines 4-5; claim 7, lines 4-5; claim 11, line 7; claim 16, lines 1-5; claim 24, lines 5-6; claim 28, lines 3-4; claim 26, line 2; claim 31, lines 2-6; claim 32, lines 5-6;

micro-controller 14 should provide a masking function for the data address mark.[24] By way of example, if only the seven (7) most significant bits are normally detected at the same time as detecting a data address mark constructed by eight (8) bits, micro-controller 14 skips the same number of bytes as the number of the least significant bit remaining,[25] and regards the following information as data. Accordingly, even if there is an occurrence of a defect in a data address mark of one byte, the following data address mark is normally detected, thereby lowering the possibility of concluding that the drive is faulty due to non-detection of the data address mark. While the data address mark as described is constructed by two (2) bytes, it may be possible to construct the data address mark by two (2) or more bytes.

As described above, the present invention has an advantage in that when one of the data address marks recorded with different patterns is normally detected,[26] the data address mark of

---

claim 35, lines 3-5; claim 36, lines 3-5; claim 37, lines 3-5; claim 38, lines 3-6; claim 39, lines 3-6; claim 40, lines 3-6; claim 41, lines 2-5; claim 42, lines 2-5; claim 43, lines 2-4; claim 44, line 2; claim 45, line 2; claim 46, line 2; claim 47, lines 1-2; claim 48, lines 1-2; claims 49, lines 1-2; claim 50, lines 2-4; claim 51, lines 2-3; claim 52, line 2-3; claim 53, lines 3-4; and claim 54, lines 3-4.

24 Claim 5, lines 2-3; and claim 6, lines 2-3. The Board may note that claims 5 and 6 described presented these features in Appellant's originally filed application.

25 Claim 4, lines 2-4; claim 18, lines 2-3; claim 19, lines 2-3; claim 22, lines 2-3; claim 23, lines 2-3; claim 25, lines 2-4; claim 29, lines 2-4; claim 30, lines 2-3; claim 33, lines 2-4; and claim 34, lines 3-4.

26 Claim 1, lines 4-5; claim 7, lines 4-5; claim 11, line 7; claim 16, lines 1-5; claim 24, lines 5-6; claim 28, lines 3-4; claim 26, line 2; claim 31, lines 2-6; claim 32, lines 5-6; claim 35, lines 3-5; claim 36, lines 3-5; claim 37, lines 3-5; claim 38, lines 3-6; claim 39, lines 3-6; claim 40, lines 3-6; claim 41, lines 2-5; claim 42, lines 2-5; claim 43, lines 2-4; claim 44, line 2; claim 45, line 2; claim 46, line 2; claim 47, lines 1-2; claim 48, lines 1-2; claims 49, lines 1-2; claim 50, lines 2-4; claim 51, lines 2-3; claim 52, line 2-3; claim 53, lines 3-4; and claim 54, lines 3-4.

a corresponding data field is regarded as an effective value in order to maximize production yield of the disk drive otherwise impaired due to non-detection of the data address mark.

While there have been illustrated and described what are considered to be preferred embodiments of the present invention, it will be understood by those skilled in the art that various changes and modifications may be made, and equivalents may be substituted for elements thereof without departing from the true scope of the present invention. In addition, many modifications may be made to adapt a particular situation to the teaching of the present invention without departing from the central scope thereof. Therefore, it is intended that the present invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out the present invention, but that the present invention includes all embodiments falling within the scope of the appended claims.

The principles of Applicant's invention are further defined by Applicant's claims which were written in the original specification as:

1. A method for forming and processing a data address mark positioned in a data track of a magnetic disk preceding a data region in a disk drive to establish synchronization [27] requested for reading user data from the magnetic disk, said method comprising the steps of:

recording of said data address mark in at least two different recording locations of said data track; and

when one data address mark recorded in said different recording locations of said data

---

[27] Claim 1, lines 2 and 7; claim 31, line 2; claim 47, line 2; claim 48, line 2; and claim 49, line 2.

track is normally detected to establish synchronization [28] requested for reading user data from the magnetic disk, regarding said one data address mark as an effective data address mark of a corresponding data region.

2. The method of claim 1, further skipping a remaining data address mark recorded in said different recording locations of said data track, when any one data address mark recorded in said different recording locations is normally detected.

3. The method of claim 2, further comprised of each of said data address mark recorded in said different recording locations of said data track being constructed of one byte of information.

4. The method of claim 3, further comprised of bits constructing said one byte being utilized for recording said data address mark and for counting the number of byte of said remaining data address mark.

5. The method of claim 1, further comprised of said data address mark being detected by a controller of said disk drive performing a masking function with respect to said data address mark.

6. The method of claim 4, further comprised of said data address mark being detected by a controller of said disk drive performing a masking function with respect to said data address mark.

---

[28] Claim 1, lines 2 and 7; claim 31, line 2; claim 47, line 2; claim 48, line 2; and claim 49, line 2.

7. A method for forming and processing a data sector comprising an identification field and a data field in a magnetic disk of a headerless servo recording system, comprising the steps of:

recording a data address mark, during a recording mode, in at least two different locations of said data field immediately preceding a data area containing user data;

detecting said data address mark recorded in said different locations of said data field, during a reading mode, to confirm validity of user data contained in said data area following said data address mark; and

when said data address mark recorded in at least one of said different locations of said data field is detected, regarding said one data address mark as an effective data address mark of a corresponding data area for confirming the validity of user data contained therein.

8. The method of claim 7, further skipping a remaining data address mark recorded in said different recording locations of said data track, when said data address mark recorded in said at least one of said different recording locations is detected.

9. The method of claim 7, further comprised of each of said data address mark recorded in said different recording locations of said data field being constructed of one byte of information.

10. The method of claim 7, further comprised of said identification field comprising an identification preamble, an identification address mark, an identification area for providing said identification information, a cyclic redundancy code, and an identification postamble.

11. A disk drive, comprising:

a data recording disk having a plurality of concentric tracks, each track having servo sectors in which servo information for use in positioning a transducer head is written and succeeding data sectors, each data sector including:

an identification region in which identification information for use to identify the data sector for reading and writing operations is written;

at least two different data address mark regions for use to indicate a validity of data recorded on said data sector is written;

a data region in which data transferred from an external communication device is written; and

an error correction code region in which an error correction code for use to automatically correct an error is written;

said transducer head for writing data to and reading data from the data sectors of the data recording disk, and for reading servo position information from the servo sectors of the data recording disk; and

means attached to the transducer head for positioning the head across the tracks to perform said read and write operations.

12. The disk drive of claim 11, further comprised of said transducer head detecting data address marks recorded in at least two different data address mark regions of said data field, during said reading mode, to confirm validity of user data contained in said data area following said data address mark, and when at least one data address mark recorded in said two different data address mark regions of said data field is detected, regarding said one data address

mark as an effective data address mark of a corresponding data area for confirming the validity of user data contained therein.

13. The disk drive of claim 11, further comprised of said transducer head skipping a remaining data address mark recorded in said different recording locations of said data track, when a data address mark recorded in said two different data address regions is detected.

14. The disk drive of claim 11, further comprised of each data address mark recorded in said two different data address mark regions of said data field being constructed of one byte of information.

15. The disk drive of claim 11, further comprised of said identification field comprising an identification preamble, an identification address mark, an identification area for providing said identification information, a cyclic redundancy code, and an identification postamble.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claim Rejection Under 35 U.S.C. §112

A. Claims 32-34 and 50-52 are rejected under the first paragraph of 35 U.S.C. §112 as failing to comply with the *written description* clause.

The Examiner contends that the claims contain the limitation "a controller regulating movement of said head based on at least one of said first data address mark and said second data address mark" which was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor, at the time the application was filed, had possession of the claimed invention.

B. Claims 32-34 and 50-52 are rejected under the first paragraph of 35 U.S.C. §112 for lack of enablement.

The Examiner contends that the specification, while being enabling for reading first and second data address marks, does not reasonably provide enablement for "a controller regulating movement of said head based on at least one of said first data address mark and said second data address mark."

Claim Rejection Under 35 U.S.C. §102(e)

C. Claims 1-3, 6, 16-17, 20-21, 24, 26-28, 31, 35-49 and 54 are rejected under 35 U.S.C. §102(e) as being anticipated by Malone Sr., U.S. Patent № 6,181,497.

The Examiner contends that Figures 2A, 5A-8, and 10 of Malone, Sr. '497 meet all the

limitations of claims 1, 16, 20, 24, 26-27, 31, 37, 40, 44, 46-47, 49, and 54.

Claim Rejection Under 35 U.S.C. §103(a)

D. Claims 7-15 are rejected under 35 U.S.C. §103(a) as being unpatentable over the proposed combination of what the Examining Staff asserts is Appellant's Admitted Prior Art modified according to Malone Sr. '497.

Claim Rejection Under 35 U.S.C. §251

E. Claims 16-54 are rejected under 35 U.S.C. §251 as being an improper recapture of broadened claimed subject matter surrendered in the application for the patent upon which the present reissue is based.

The Examiner contends that a broadening aspect, which was not present in the application for patent, is present in the reissue application, and that the broadening aspect in the reissue application relates to the subject matter which Appellant previously surrendered during the prosecution of the application.

VII. ARGUMENT

A. Rejection of claims 32-34 and 50-52 Under the *Written Description* Clause of the First Paragraph of 35 U.S.C. §112

Claims 32 through 34 and 50 through 52 are finally rejected under the first paragraph of 35 U.S.C. §112 as failing to comply with the written description requirement. Specifically, the Examining staff contends that the specification fails to describe "a controller regulating movement of said head based on at least one of said first data address mark and said second data address mark." This rejection is unfounded, is improper and should be withdrawn.

1. The Examining Staff Has Failed To Consider The Clear Support And Antecedent Basis For The Claims That Is Set Forth In Appellant's Originally Filed Specification

Specifically, the Examiner states that the specification fails to describe,

> "a controller regulating movement of said head based on at least one of said first data address mark and said second data address mark." [29]

Appellant's specification complies with 37 CFR §1.75(d)(1), which states that,

> "the terms and phrases used in the claims must find clear support **or** antecedent basis in the description so that the meaning of the terms in the claims may be ascertained by reference to the description."

Here, the Examining staff has failed to identify any term or any phrase as lacking either "clear support" or as lacking "antecedent basis." Second, the Examining staff has failed to identify any inability to ascertain the meaning of the cited passage of the claims.

---

[29] Claim 32, lines 5 and 6; claim 50, lines 5 and 6; claim 51, lines 4 and 5; and claim 52, lines 5 and 6.

2. The Examining Staff Has Failed To Consider The Clear Support And Antecedent Basis For The Claims That Is Set Forth In Appellant's Originally Filed Specification For Each Element Set Forth In Claims And For The Relationship Between Those Elements Defined By Those Claims

In Paper № 20060328, the Examining staff questions whether Appellant's specification fails to describe,

> "a controller regulating movement of said head based on at least one of said first data address mark and said second data address mark." [30]

As is demonstrated by the following excerpts taken from Appellant's originally filed specification, that specification provides either "clear support" or "antecedent basis" for both of the elements introduced by this paragraph of the claims and for the relationship that exists between these elements. More specifically, Appellant's specification expressly states that,

> "a high density hard disk drive HDD constructed according to the principles of the present invention ... includes, for example, ... corresponding four transducer heads 4, a transducer head assembly 6 in an E-shape having actuator arms 5 each for supporting a respective pair of transducer heads 4, a preamplifier 8, a read/write channel circuit 10, an analog-to-digital (A/D) converter 12, a track information detector 13, a micro-controller 14, a digital-to-analog (D/C) converter 16, a voice coil motor (VCM) driver 18, a voice coil motor 20 ... and a disk data controller (DDC) 28."[31]

Appellant then teaches:

> "Preamplifier 8 is electrically connected to the transducer head assembly 6 for amplifying a predetermined signal read out from

---

[30] Claim 32, lines 5 and 6; claim 50, lines 5 and 6; claim 51, lines 4 and 5; and claim 52, lines 5 and 6.

[31] Son' 387, column 4, lines 53-68 and column 5, lines 1-3.

> the disk 2 using the transducer head 4 and transmitting the amplified signal to the read/write channel circuit 10."[32]

Appellant's original specification additionally teaches that:

> "Read/write channel circuit 10 is connected between the preamplifier 8 and the DDC 28 for decoding data pulses from an input signal received from the preamplifier 8 to generate read/out data RDATA ... ."[33]

The specification continues to explain that:

> "Track information detector 13 is connected between the read/write channel circuit 10 and the micro-controller 14 for detecting from the RDATA, a track number for the current position of the transducer head 4 and providing the detected data to the micro-controller 14. The DDC 28 is controlled by the micro-controller 14 to record the data received from a host computer via the read/write channel circuit 10 and the preamplifier 8 or to transmit the data read out from the disk 2 to the host computer."[34]

The specification further explains that:

> "Micro-controller 14 controls the DDC 28 according to a command received from the host computer to search a track and position of the transducer head. In doing so, the micro-controller 14 uses the track number and the PES input from the track information detector 13 and the A/D converter 12, respectively. The D/A converter 16 is connected to the micro-controller 14 for converting the digital signal output from the micro-controller 14 into an analog signal for controlling the position of the transducer heads 4. A VCM driver 18 generates a driving current for driving a VCM 20 according to the analog signal input from the D/A converter 16. The VCM 20 drives the transducer heads 4 to move

---

32 Son' 387, column 5, lines 4-8.

33 Son' 387, column 5, lines 14-19.

34 Son' 387, column 5, lines 29-37.

> in a radial direction of the disk 2 corresponding to the level of the driving current input from the VCM driver 18."[35]

Appellant's original specification states that,

> "[t]he two data address marks are respectively distinguished by using different patterns, and is discriminated by the micro-controller 14." [36]

With a data field, such as may be used with a headerless servo recording system, the:

> "data address mark informs that the data is started and provides necessary synchronization when the magnetic disk driving apparatus reads the data. ... if there is occurrence of a defect in the data address mark area, it is difficult if not impossible to restroe the damaged data address mark. As a result, since the data address mark is not detected, data positioned at the data area following the data address cannot be normally accessed." [37]

It may be seen from the foregoing litany of excerpts from the "description" set forth in Appellant's originally filed application, that not only has the Examining staff failed to identify any term or any phrase as lacking either "clear support" or lacking "antecedent basis" in Appellant's original specification, but that the original specification fully complies with the *written description* requirement of the first paragraph of 35 U.S.C. §112, as evidenced by Appellant's compliance with 37 CFR §1.75(d)(1), by describing a structure that regulates movement of one, or more heads, and a structure that regulates movement of one, or more heads based upon one or more of the first data address mark and the second data address mark, provides both "clear support" **and** "antecedent basis" for both of the elements introduced by

---

35 Son' 387, column 5, lines 38-51.

36 Son '387, column 5, lines 64-67.

37 Son '387, column 4, lines 35-51.

this paragraph of the claims and for the relationship that exists between these elements because absent regulation of the movement based upon the first data address mark and the second data address mark, reading of data sought by the host computer is problematical, as is explained by Appellant's original specification.

3. The Examining Staff Has Failed To Consider The Entirety Of Clear Support And Antecedent Basis For The Rejected Claims That Is Set Forth In Appellant's Originally Filed Specification

In essence, this rejection under the *written description* requirement of the first paragraph of 35 U.S.C. §112 questions Appellant's definition of its disk "controller" with the clause "regulating movement of said head based on at least one of said first data address mark and said second data address mark."[38] Under the first paragraph of 35 U.S.C. §112 and 37 CFR §1.75(d)(1), the meaning of the terms in claims may be ascertained by reference to the description." There is no requirement under either the first paragraph of 35 U.S.C. §112 or 37 CFR §1.75(d)(1) that the specification provide a tutorial for every noun and verb which appears in the claims. Here, Appellant's specification provides clear disclosure as the import of every term used in the claims, that is, for each of the terms *a controller*, *regulating movement of the head*, and *based on at least one of said first data address mark and said second data address mark*.[39]

***i.* "A controller"**

As is explained in Appellant's specification,

---

[38] Claims 32 through 34 and 50 through 52.

[39] *Manual of Patent Examining Procedure*, 8th Ed., Rev. 3 (August 2005), §806.01(o).

> "Micro-controller 14 controllers the DDC 28 according to a command received from the host computer to search a track and position of the tranducer head. In doing so, the micro-controller 14 uses the track number and the PES input from the track information detector 13 and the A/D converter 12, respectively."[40]

This explanation of Appellant's "controller" is in conformance with the use of that term in the art, one exemplar of which states,

> "**Controller:** Sometimes referred to as an *interface*, or *storage controller*. The controller, which is attached to the computer, decodes instructions from the computer and issues instructions to the *disk drive* to do what the computer has instructed. The controller also receives data and status information from the disk drive, which it passes to the computer in a form [*sic*, that] the computer can understand."[41]

Neither Paper № 20051109 nor Paper № 20060328 make any allegation that the meaning of Appellant's "controller" is not "apparent from the descriptive portion of the specification"

ii. **"Regulating movement of the head"**

The *RAMAC* is well known in the art as the "first hard-disk storage."[42] Two characteristics of the *RAMAC* was that "it was always running" and that it used "two moving 'heads' that read and wrote information."[43] Appellant's specification states that,

> "Micro-controller 14 control the DDC 28 according to a command

---

40 Son '387, column 5, lines 38-43.

41 *Fragmentation: Glossary of Terms*, http://www.diskeeper.com/fragbook/glossary.htm. 31st of July 2006.

42 *The Hard Disk That Changed The Word*, – IBM delivered the first disk drive 50 years ago. It was about the size of two refrigerators and weighted a ton. *Newsweek*, 7th August 2006 issued, by Steven Levy, available from mnsnbc.msn.com.

43 *Newsweek*, 7th August 2006 issued, by Steven Levy.

> received from the host computer to search a track and ***position of the tranducer head***",[44]

and then explains that:

> "[a] VCM 20 drives the transducer heads 4 to move in a radial direction of the disk corresponding to the level of the driving current input from the VCM driver 18."[45]

Recognizing that Appellant teaches that,

> "[t]he data address mark informs that the data is started and provides necessary synchronization when the magnetic disk driving apparatus reads the data",[46]

the data address marks in point of fact, relies upon the *data address mark* to *regulating movement of the head.* The Examining staff is reminded that regulation of the heads is continuous and that the typical protocol governing operation of a hard disk drive is to either continue or to repeating the search until a default condition occurs (*e.g.*, an excessive number of search cycles has been completed without locating a recognizable data address mark. This explanation by Appellant's specification is consistent with both the definition of Appellant's "controller" by claims 32 through 34 and 50 through 52 as "regulating movement of the head" and with the fifty years of progress in the hard disk art beginning with the *RAMAC.*

iii. **"Based on at least one of said first data address mark and said second data address mark"**

Both characteristics of the *RAMAC*, namely that that "it was always running" and that

---

[44] Son '387, column 5, lines 38-43.

[45] Son '387, column 5, lines 46-49.

[46] Son '387, column 4, lines 35-37.

it used "moving 'heads' that read and wrote information"[47] have remained common to hard disk drives in the subsequent fifty years. As was explained by a later author,

> "The two primary objects of a head positioning system are (1) to maintain the head at or very near the track centerline while writing or reading and (2) to move the head rapidly from one track to another so as to minimize the time taken to locate the head at or near the centerline of the target track. The latter function is known as "seeking."[48]

For various reasons, some related to mechanical aspects (*e.g.*, harmonics and vibrations of the armature arm relative to the frame of the hard disk drive), some related to electrical aspects (*e.g.*, the fact that the electrical current fed to the voice coil motor is typically used to position the armature arm, creates a force or torque with is proportional to that current), and some of which are environmental (*e.g.*, temperature, external shock or externally induced vibrations), one problem that existed at the time of Appellant's invention,

> "with current head positioning systems is the impairment of settling time ... ."[49]

Settling time is that period "at the end of a seek" when "the head must 'settle." These problems in the art resulted "in an extended seek time"[50] and required that such "post seek motions" be addressed before data could be read or written. Appellant's original specification describes that regulation of the head during the seek time includes more than a single step of initiating a

---

47 *Newsweek*, 7th August 2006 issue, by Steven Levy.

48 U.S. Patent № 5.510.939 for *Disk Drive With Adaptive Positioning* to M. M. Lewis, 23rd of April 1996, column 1, lines 37-43.

49 U.S. Patent № 5.510.939 to M. M. Lewis, column 2, lines 20 and 21.

50 U.S. Patent № 5.510.939 to M. M. Lewis, column 2, lines 35 and 36.

movement of a head.[51] In particular, Appellant's specification states that,

> "In contemporary HDD using the headerless recording format, if there is occurrence of a defect in the data area, *damaged data can be restored* by using the ECC. If there is an occurrence of a defect in a data address mark however, *it is difficult or impossible to restore* the damaged data address mark. As a result, *since* the data address mark is not detected, data positioned at a rear area following the data address mark *cannot normally be accessed.*"[52]

Recognizing that "micro-controller 14 controls the DDC 28 ... to search a track and position of the transducer head,

> "during the read operation of each sector, when only one byte of data address mark is detected among 2 bytes of data address marks, it is regarded as an effective data address mark. ... If it is determined whether the second data address mark is normally detected, the following information is regarded as data. ... Meanwhile, the micro-controller 14 should provide a masking function for the data address mark."[53]

In broader language, the head reads a "data address mark" and micro-controller 14 and DDC 28 respond "according to a command received from the host computer to search a track and position of the transducer head" by "controlling the position of the transducer heads 4."[54] Once the:

> "data address mark informs that the data is started and provides

---

51 Under current practice, it is not the current policy of the Office that the language of the claims be repeated *ipsa verbis* within the specification; it is the policy of the Office that "the terms and phrases used in the claims must find clear support **or** antecedent basis in the description **so that the meaning of the terms in the claims may be ascertained** by reference to the description." 37 CFR §1.75(d)(1).

52 *Son* '387, column 3, lines 9-14.

53 Son '387, column 6, lines 5-19.

54 Son '387, column 5, lines 38-43.

> necessary synchronization when the magnetic disk driving apparatus reads the data." [55]

When the head has read data from that particular sector addressed during that read operation,

> "[m]icro-controller 14 controls the DDC 28 according to ... [the next] command received from the host computer to search ... [another] track and position of the tranducer head [on that track]",[56]

which is simply a repetition of the previous step in the read operation described throughout column 4 through 6 of Appellant's specification. Throughout the "seek time" however, and until the:

> "data address mark informs that the data is started and provides necessary synchronization when the magnetic disk driving apparatus reads the data." [57]

Appellant's use of "a controller" to regulate "movement of said head" continues until the:

> "data address mark informs that the data is started and provides necessary synchronization when the magnetic disk driving apparatus reads the data." [58]

In summary, for the fifty years since the *RAMAC* first spun on its axis, hard disk drives have been "always running", that is, always the hard disk has been continuously rotating, and "a controller" has always sought throughout the "seek time":

> "(1) to maintain the head at or very near the track centerline while writing or reading and (2) to move the head rapidly from one track

---

55 Son '387, column 4, lines 36-38

56 Son '387, column 5, lines 38-43.

57 Son '387, column 4, lines 36-38

58 Son '387, column 4, lines 36-38

> to another so as to minimize the time taken to locate the head at or near the centerline of the target track."[59]

This may only be done by "regulating movement of said head" and this use of "a controller regulating movement of said head" is performed, at least in part after the completion of "seek time" associated with a corresponding "command from the host computer to search a track and position of the transducer head ... [and thereby] controlling the position of the transducer heads 4",[60] "based on at least one of said first data address mark and said second data address mark"[61] informing "that the data is started ...", thereby ending one iteration of a read operation. Consequently, during each "read operation", Appellant's "controller" regulates "movement of said head based on [at least during one portion of the read operation] at least one of said first data address mark and said second data address mark"[62] in the precise manner described in Appellant's originally filed specification.

Due to fragmentation of the storage of user data throughout different sectors and on different tracks, each iteration of a read operation must be repeated, albeit with a different,

> "command received from the host computer to search ... [another] track and position of the transducer head [on that track]",[63]

once the:

> "data address mark informs that the data is started and provides

---

59 U.S. Patent № 5.510.939 for *Disk Drive With Adaptive Positioning* to M. M. Lewis, 23rd of April 1996, column 1, lines 37-43.

60 Son '387, column 5, lines 38-46.

61 Claims 32-34 and 50-52.

62 Claims 32-34 and 50-52.

63 Son '387, column 5, lines 38-43.

> necessary synchronization when the magnetic disk driving apparatus reads the data", [64]

indicates completion of the preceding iteration. Appellant submits therefore, that the foregoing demonstration establishes that from Appellant's specification **"the meaning of the terms in the claims may be ascertained** by reference to the description" as is contemplated by 37 CFR §1.75(d)(1). The Board is urged to refuse to sustain this rejection.

The Examining staff is respectfully invited to consider the three operational scenarios described in the foregoing excerpts taken from the written description of Appellant's original specification invoking the structure defined by claims 32 through 34 and 50 through 52. In the first of these two scenarios,

> "[d]uring the read operation of each section, when only one byte of data address mark is detected among 2 bytes of data address marks, it is regarded as an effective data address mark. That is, if the first data address mark is normally detected, the second data address mark of one byte is skipped and the following information is regarded as data." [65]

This first scenario expressly contemplates movement of the head 4, and in the larger scheme of the operation of the disk drive, movement of the magnetic head 4 must continue after reading of the first data address mark if, for no other reason than to pass over (or "skip") the second data address mark and place head 4 in a position relative to the disk so that head 4 is able to read the data stored after the second data address mark; regulation of that movement by, *inter alii*, a component such as a controller 14. In consideration of this first scenario, the Examining

---

[64] Son '387, column 4, lines 36-38

[65] Son '387, column 5, lines 38-46.

staff has not sought to deny that Appellant's teaching of regulation of the movement of head 4 to accommodate movement of head 4 to a position which would allow head 4 to read the first data address mark does, in point of fact, constitute "regulating movement of said head based on at least one of said first data address mark and said second data address mark"? [66]

In the second scenario Appellant's specification states that,

> "[d]uring the read operation of each section, when only one byte of data address mark is detected among 2 bytes of data address marks, it is regarded as an effective data address mark. That is, if the first data address mark is normally detected, the second data address mark of one byte is skipped and the following information is regarded as data. If the first address mark has a defect, however, the second data address mark is detected." [67]

In other words, when difficulty, for whatever reason, including "[w]hen the first address mark has a defect," [68] is encountered in when seeking to detect the first address mark, Appellant's "controller" must make a determination of whether "the first data address mark" has been normally detected and a second determination must be made to attempt to detect the second address mark; this second scenario necessarily contemplates continued regulation and movement of head 4,[69] and in the larger scheme for operation of the disk drive, movement of

---

66 As an aside, it may be noted that the "skipping" of the second data address mark may be accomplished in more than one way, and as Appellant's claims are presented, is not limited to a physical or software implemented step. By way of example, the specification explains that "micro-controller 14 should provide a masking function for the data address mark." Column 6, lines 17-19.

67 Son '387, column 6, lines 5-11.

68 Son '387, column 6, lines 5-11.

69 In point of fact, it is the reading, or inability to read, which is the impetus for continued regulation and continued movement of the head and disk that is precisely what Malone '497 teaches when he is unable to read his *primary sync bytes*. Specifically,

magnetic head 4 must continue after reading of the second data address mark if, for no other reason than to position head 4 in a position relative to the disk so that head 4 is able to read the data stored after the second data address mark; regulation of that movement will be made by, *inter alii*, a component such as a controller 14. In consideration of this second scenario, the Examining staff is respectfully requested to contemplate whether regulation of the movement of head 4 to accommodate movement of head 4 to a position which would allow head 4 to read the second data address mark would constitute "regulating movement of said head based on at least one of said first data address mark and said second data address mark"?

In the third scenario, neither the first nor the second data address mark are able to be detected upon the first pass of head 4. The Examining staff is respectfully invited to contemplate whether regulator 14, or some other controller such as a host computer, might continue to regulate movement of head 4 based upon one, or perhaps both, of the first data address mark and the second data address mark in the third scenario. Could regulation of the movement of head 4 to accommodate a second pass by head over the first data address mark would constitute "regulating movement of said head based on at least one of said first data address mark and said second data address mark"? Could regulation of the movement of head 4 to accommodate some alternative default movement by the head constitute "regulating movement of said head based on at least one of said first data address mark and said second data address mark"?

"According to this first embodiment, if a primary sync byte field is unreadable, an error recovery procedure is invoked and the channel **attempts a read** of the secondary sync bytes **on a subsequent revolution**. Page 9, lines 14-17." Amendment filed by Malone '497 on the 25th of January 1999, page 2. Copy attached.

Accordingly, an in view of the foregoing demonstration that Appellant's specification does in fact give "clear support **or** antecedent basis in the description so that the meaning of the terms in the claims may be ascertained by reference to the description", there is no basis for maintaining this rejection under the *written description* clause of the first paragraph of 35 U.S. §112. The Board is respectfully urged to refuse to sustain this rejection.

B. The Rejection of claims 32-34 and 50-52 Under the *Written Description* Clause is premised upon an improper application of the First Paragraph of 35 U.S.C. §112

In support of this rejection of claims 32 through 34 and 50 through 52 under the first paragraph of 35 U.S.C. §112 as failing to comply with the *written description* clause, the Examining Staff contends that,

> "a controller regulating movement of said head based on at least one of said first data address mark and said second data address mark" which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention."

Paper № 20060328 continues by stating that,

> "There is no disclosure of regulating movement of the head based on one of the data address marks as claimed. Col. 4, lines 5-11 show the disk format is servo sectors and data sectors, and the actual digital data is written into the data fields which are in the data sectors, not the servo sectors. Col. 4, lines 26-30 and 34-37 show the data address mark is part of the data field, the data address mark informs that the data is started and provides necessary synchronization when reading the data, and the data is the actual digital information stored in the disk, and thus is not the servo information stored on the disk in the servo sector. Col. 4, lines 12-21 do discuss information such as cylinder number which could conceivably be used while regulating movement of said head, but this is in the context of the ID field, which is distinct

> from the data field. Col. 5, lines 21-43 describe regulating movement of said head, but by using head position information which is servo information, and by using a track number. The disclosure does not state the source of the track number information. A review of all the prior art cited by both the examiner and by Appellant during the prosecution of this application shows track number information is commonly obtained in the art from the servo information in servo sectors, not from the user data in data sectors. Even if it were obtained from the cylinder number mentioned above, that would still be from the ID field and not from the data field. There is no description of said claim limitation in Appellant's disclosure as originally filed, thus said claim limitation is new matter and must be deleted from the claims.

Appellant suggest that the Examining staff has misinterpreted the first paragraph of 35 U.S.C. §112. "The invention" referred to by the first paragraph is defined by the second paragraph of 35 U.S.C. §112, in which the Congress of these United States has granted exclusively to "the Appellant", and not to the Examining staff, the sole right to determine "the subject matter which the Appellant regards as his invention." Appellant has exercised that right, and has specifically defined certain aspects in the rejected claims; nothing in the claims at issue restricts the practice of the subject matter which Appellant regards as his invention to regulating movement of a head on the basis of only "information such as cylinder number which could conceivably be used while regulating movement of said head," or upon information read from "the ID field, which is distinct from the data field." Moreover, nothing in the rejected claim requires the regulation of movement to be based upon "information such as cylinder number" or upon "the ID field." The attention of the Examining staff is invited to consider that the questioned paragraphs of the rejected claims do not assert that the data address marks contain "the servo information stored

on the disk in the servo sector" as asserted by the Examining staff; as is demonstrated throughout the foregoing pages of this paper in response to the objection to the specification, the specification provides a clear, written description of the subject matter which the Appellant regards as his invention. As one item of evidence of record, the Examining staff is again invited to contemplate Appellant's three operational scenarios invoking the structure described in the originally filed specification. In the first of the scenarios,

> "[d]uring the read operation of each section, when only one byte of data address mark is detected among 2 bytes of data address marks, it is regarded as an effective data address mark. That is, if the first data address mark is normally detected, the second data address mark of one byte is skipped and the following information is regarded as data." [70]

The first scenario expressly contemplates movement of the head 4, and in the larger scheme of the operation of the disk drive, movement of the magnetic head 4 must continue after reading of the first data address mark if, for no other reason than to pass over (or "skip") the second data address mark and place head 4 in a position relative to the disk so that head 4 is able to read the data stored after the second data address mark; regulation of that movement by, *inter alii*, a component such as a controller 14. In consideration of this first scenario, the Examining staff is respectfully requested to contemplate whether regulation of the movement of head 4 to accommodate movement of head 4 to a position which would allow head 4 to read the first data address mark would constitute "regulating movement of said head based on at least one of said

[70] Son '387, column 6, lines 5-11.

first data address mark and said second data address mark"? [71]

In the second scenario,

> "[d]uring the read operation of each section, when only one byte of data address mark is detected among 2 bytes of data address marks, it is regarded as an effective data address mark. That is, if the first data address mark is normally detected, the second data address mark of one byte is skipped and the following information is regarded as data. If the first address mark has a defect, however, the second data address mark is detected." [72]

In other words, when difficulty is encountered in detecting the first address mark, one determination must be made of whether "the first data address mark" has been normally detected and a second determination must be made to attempt to detect the second address mark; this second scenario expressly contemplates movement of the head 4, and in the larger scheme for operation of the disk drive, movement of the magnetic head 4 must continue after reading of the second data address mark if, for no other reason than to position head 4 in a position relative to the disk so that head 4 is able to read the data stored after the second data address mark; regulation of that movement will be made by, *inter alii*, a component such as a controller 14. In consideration of this second scenario, the Examining staff is respectfully requested to contemplate whether regulation of the movement of head 4 to accommodate movement of head 4 to a position which would allow head 4 to read the second data address mark would constitute "regulating movement of said head based on at least one of said first data address mark and said

---

[71] As an aside, it may be noted that the "skipping" of the second data address mark may be accomplished in more than one way, and as Appellant's claims are presented, is not limited to a physical or software implemented step.

[72] Son '387, column 6, lines 5-11.

second data address mark"?

In the third scenario, neither the first nor the second data address mark are able to be detected upon the first pass of head 4. The Examining staff is respectfully invited to contemplate whether regulator 14, or some other controller such as a host computer, might continue to regulate movement of head 4 based upon one, or perhaps both, of the first data address mark and the second data address mark in the third scenario. Could regulation of the movement of head 4 to accommodate a second pass by head over the first data address mark would constitute "regulating movement of said head based on at least one of said first data address mark and said second data address mark"? Could regulation of the movement of head 4 to accommodate some alternative default movement by the head constitute "regulating movement of said head based on at least one of said first data address mark and said second data address mark'"?

Accordingly, an in view of the foregoing demonstration that Appellant's specification does in fact "contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable ... ." There is therefore, no basis for maintaining this rejection of claims 32 through 34 and 50 throuigh 53 under the written description clause of the first paragraph of 35 CFR §112. The Board is therefore, respectfully urged to refuse to sustain this rejection.

C. Rejection of Claims 32-34 and 50-52 Under the *Enablement* Clause of the First Paragraph Of 35 U.S.C. §112

Claims 32 through 34 and 50 through 52 were rejected in Paper Nos. 20051109 and 20060328 under the **first** paragraph of 35 U.S.C. §112 as "being enabling for reading first and second data address marks, does not reasonably provide enablement for ***a controller regulating movement of said head based on at least one of said first data address mark and said second data address mark.***" Appellant respectfully traverses this rejection for the following reasons.

Contrary to the assertion of the Examining staff, the paragraph of the rejected claims in question do not contain the verb "reading." Pending claims 32, 50, 51 and 52 read, in part:

> "a controller regulating movement of said head based on at least one of said first data address mark and said second data address mark."

Turning again to the Examiner's stated concern,

> "The disclosure does not state the source of the track number information. A review of all the prior art cited by both the examiner and the Appellant during prosecution of t his application shows ***it*** is commonly obtained in the art from the servo information in servo sectors, not the user data in data sectors. Even if it were obtained from the cylinder number mentioned above, that would still be form the ID field and not from the data field."[73]

and the Examiner's summary conclusion that,

> "making the claimed invention would require undue experimentation, as the disclosure completely lacks any description of how one can regulate the position of the head based on data address marks, while the cited prior art fails to show even

[73] Paper Nos. 20051109 and 20060328, page 4.

> the slightest description of how this ***feat*** can be performed and the examiner in his experience can not recall any showing in the prior art of ***such a means*** for regulating head movement."[74]

Appellant respectfully submits that this rejection couched upon a question of "enablement" is simply a rewording of the conclusion set forth in Paper Nos. 20050510 and 20060328, namely that "the word 'movement' renders the claim indefinite."[75] The issue here is not the presence, or absence, of regulation of *movement*, but synchronization in the regulation of that movement. In the art of synchronization of a clock to read data from a storage medium, the actual format of a *data track* depends upon the particular design of the disk drive system.[76] Regardless of format however, "the electronics controlling the storage and retrieval operations of a disk drive must have the means to precisely and reliably determine the *start of user data* in each data sector so that data may be accurately reproduced."[77]

This ***movement*** of the actuator assembly is controlled by the servo electronics and servo microcode, "which regulate a control signal to a voice coil motor."[78] Closed loop servo systems use,

---

74 Paper Nos. 20051109 and 20060328, pages 4 and 5.

75 Paper Nos. 20051109 and 20060328, pages 4 and 5.

76 As explained by Malone '497, *infra*, "[d]ata tracks are further subdivided into one or more blocks or sectors of data." Column 1, lines 19-21.

77 See, by way of example of the state of synchronization in the art, Daniel J. Malone, U.S. Patent № 6.181.497 issued 30 January 2001; Daniel J. Malone, U.S. Patent № 6.124.994 issued 26 September 2000; Daniel J. Malone, U.S. Patent № 6.392.830 issued 21 May January 2002; and Daniel J. Malone, U.S. Patent № 6.583.943 issued 24 June 2003, all at column 1, lines 21 through 26.

78 Malone '497, column 1, lines 44-46.

> "feedback information [read] from the disk to find and maintain a position over a target track."[79]

As is explained by Malone '497, the:

> "feedback information may be [either] located on a signal, dedicated disk surface (*i.e.*, a dedicated servo) or embedded on data tracks between portions of data (embedded servo)."[80]

Malone '497 carefully distinguishes between servo information such as AGC recovery field 10, clock synchronization or VFO field 12, and sync byte field 14 including one or more adjactnt sync bytes, and the user defined data found in data field 16, and nowhere attributes any servo function to the data. Appellant's "data address mark" however, is a constituent component of a "data field."[81] As is explained by Appellant's original specification, the:

> "data address mark informs the disk drive that the data is started and provides necessary synchronization when the magnetic disk driving apparatus reads the data."[82]

This is what is expressly taught by Appellant's specification when the Appellant writes that the:

> "data address mark informs the disk drive that the data is started and provides necessary synchronization when the magnetic disk driving apparatus reads the data."[83]

How the servo circuit may be designed to employ the synchronization component of a data address mark is a separate issue, but it is important to recall that Appellant's microcontroller

---

79 Malone '497, column 1, lines 46-48.

80 Malone '497, column 1, lines 48-51.

81 Son, U.S. Patent № 5.963.387 issued 5 October 1999, column 4, lines 26 and 27.

82 Son '387, column 4, lines 35-37.

83 Son '387, column 4, lines 35-37.

14 receives:

- "a phase error signal (PES)" generated by read/write by "decoding head position information, *i.e.*, a part of servo information, which is recorded on the disk ... The PES is then transmitted to the micro-controller 14 via the A/D converter 12. At this stage the A/D converter 12 converts the PES into a digital value corresponding to a predetermined level and transmits the converted PES to the micro-controller 14."[84]

- "Track information detector 13 is connected between the read/write channel circuit 10 and the micro-controller 14 for detecting from the RDATA, a track number for the current position of the transducer head 4 and providing the detected data to the micro-controller 14.[85]

- Micro-controller 14 controls the DDC 28 controls the DDC 28 according to a command received from the host computer to search a track and *position* of the transducer head. In doing so, the micro-controller 14 uses the track number and the PES input *from* the track information detector 13 *and* the A/D converter 13, respectively."[86]

---

84 Son '387, column 5, lines 21-28.

85 Son '387, column 5, lines 29-33.

86 Son '387, column 5, lines 38-43.

Accordingly, Appellant's "controller regulating movement of a data address mark in controlling movement and maintaining track alignment of the head based on at least one of said first data address mark and said second data address mark" is not indefinite. The Board is respectfully urged to refuse to sustain this rejection.

D. Rejection of Claims 1-3, 6, 16, 17, 20, 21, 24, 26-28, 31, 32, 35-51 and 54 under 35 U.S.C. §102(e)

Claims 1 through 3, 6, 16, 17, 20, 21, 24, 26 through 28, 31, 32, 35 through 51 and 54 are finally rejected under 35 U.S.C. §102(e) as being anticipated by Malone Sr., U.S. Patent № 6,181,497. Thorough consideration of Malone '497 reveals that none of these claims are anticipated.

In support of this rejection, the Examiner contends that Figures 2A, 5A-8, and 10 of Malone, Sr. '497 meet all the limitations of claims 1, 16, 20, 24, 26, 27, 31, 37, 40, 44, 46, 47, 49, and 54; Paper Nos. 20051109 and 20060328state that,

> "Malone, Sr. Figures 2A, 5A-8, and 10 meet all [of] the limitations of claims 1, 16, 20, 24, 26-27, 31, 40, 44, 46-47, 49, and 54. Figure 5A shows recording said data address mark to establish synchronization requested for reading user data in at least two different recording locations (14 and 62, where sync bytes correspond to the claimed data address marks as they indicate the location of the data along the track), and Figure 8 shows when one data address mark (14) is detected (92) to establish synchronization requested for reading user data (96), regarding said one mark as an effective mark of a corresponding data region, and skipping a remaining mark (62) when any one mark is normally detected (98), which comprises distinguishing between the two address marks. Figure 2A shows data blocks (34) preceding said servo information area (30)."

This excerpt taken from Paper Nos. 20050510 and 20060328, given by the Examining staff as its rationale for finding anticipation, fails to make a *prima facie* showing of anticipation under 35 U.S.C. §102(e) and is unsupported by the teachings of Malone U.S. Patent № 6.181.497 issued on the 30th of January 2001.

1. **The Examining Staff Has Failed To Correctly Read Malone '497**

Malone '497 has stated that,

> "The present application describes a "redundant sync byte field" as follows:
>
> As noted previously, the primary objective of the invention is to provide a data block format that provides a redundant sync byte field sufficiently spaced from the primary sync byte field to assure the readability of data despite the occurrence of disk defects spanning multiple bytes. Page 17, lines 8-12.
>
> According to this first embodiment, if a primary sync byte field is unreadable, an error recovery procedure is invoked and the channel attempts a read of the secondary sync bytes on a subsequent revolution. Page 9, lines 14-17.
>
> In contrast Leis describes:
>
> The preamble 32 is used to set the gain of the AGC 20 and to lock the phase of the PLL 16 to the bit frequency and phase of the header. Col 4, lines 60-63.
>
> Thus Leis describes preamble 32 as being used to synchronize to the frequency and phase of the header 28A and not to synchronize to the frequency and phase of the data section 28B. Furthermore Leis describes:
> If any of the header sub-sections following the DC-erase field are not detected correctly within the predetermined times, the system looks for another DC-erase field and then continues the synchronization process. Col. 3, lines 6-9
> Thus Leis describes searching for another DC-erase field 30 if

> either preamble 32 or synch char 34 are not detected. **Leis does not** describe or suggest a "redundant sync byte field" that assures the readability of data despite the occurrence of disk defects spanning multiple bytes, as in claim 98. Furthermore, as is known by those of ordinary skill in the art servo fields, such as servo field 38 in Leis Fig. 2, are written as part of the process of manufacturing a disk drive. Whereas, data fields, including the preamble 40 and synch char 42 are written by the drive in the normal course of its operation. Thus, the preamble 32 and synch char 34 in header 28A and the preamble 40 and synch char 42 in data 28B are written at separate times. As a result there are phase differences between the two sets of fields. Hence, the preamble 32 and synch char 34 are used for reading the header 28A, and the preamble 40 and synch char 42 are used to read data 28B."[87]

In contradistinction to the express teachings of Malone '497, the Examining staff now argues that "Figure 5A shows recording said data address mark to establish synchronization requested for reading user data in at least two different recording locations (14 and 62, where *sync bytes* correspond to *the claimed data address marks* as they indicate the location of the data along the track), and Figure 8 shown [*sic*, "that"] when one data address mark (14) is detected (92) to establish synchronization requested for reading user data (96) ..." despite the fact that Malone '497 emphatically teaches that "the primary objective of the invention is to provide a data block format that provides a redundant sync byte field sufficiently spaced from the primary sync byte field to assure the readability of data despite the occurrence of disk defects spanning multiple bytes. Page 17, lines 8-12. According to this first embodiment, if a primary sync byte field is unreadable, an error recovery procedure is invoked and the channel attempts a read of the

---

[87] Malone '497, Patent № 6.181.497, Serial № 08/570.878, Amendment filed on the 25th of January 1999, pages 2 through 4.

secondary sync bytes on a subsequent revolution. Page 9, lines 14-17."[88]

2. The Anticipation Rejection Of Claims 1-3, 6, 16, 17, 20, 21, 24, 26-28, 31, 32, 35-51 And 54 Depends Upon A Technically Inaccurate Interpretation Of Malone '497

Claim 1 reads, *inter alia*,

> "recording of said data address mark in at least two different recording locations of said data track ... ."

while claim 16 reads,

> "a data block preceding a servo information area in a magnetic recording medium for accessing user data therefrom, comprising:
> writing a first data address mark in said data block; and
> writing a second data address mark in said data block at a location preceding said servo information area;

and claim 20 reads,

> "magnetic recording medium having a data track having one or more data blocks preceding a servo information area, comprising:
> a first data address mark located before said servo information area in a first data block; and
> a second data address mark located before said servo information
>
> area in said first data block."

Claim 24 reads:

> "a magnetic recording medium having at least one data block that includes at least a first data address mark and a second data address mark having no servo information area therebetween";

claim 31 reads:

> "recording a data address mark providing synchronization that

[88] Malone '497, Patent № 6.181.497, Serial № 08/570.878, Amendment filed on the 25th of January 1999, page 2.

> enables reading of data from the memory disk, along a data track on the memory disk at a first location on a first data block preceding a servo information area";

and claim 32 reads:

> "a head positioned to read, within at least one of a plurality of data blocks of a recording medium, a first data address mark, and a second data address mark, said first data address mark and said second data address mark having no servo information therebetween ... ."

One definition of an "address mark" is a "[t]wo byte address at the beginning of both the ID field and the data field of the track format";[89] claims 1 through 3, 6, 16, 17, 20, 21, 24, 26 through 28, 31, 32, 35 through 51 and 54 define, among other aspects of Appellant's inventions, storage topography and steps in terms of "data address marks." Malone '497 however, nowhere uses the phrase "data address mark." To paraphrase the Board of Patent Appeals and Interferences, how can Malone '497 be read to teach Appellant's "recording of said data address mark in at least two different recording locations of said data track " when Malone '497 does not even use the phrase "*data address mark*"?

By definition, a "servo-mark" is a component of a "feed-back positioning system" that is "needed to help [the] magnetic head to evaluate its current position."[90] Malone '497 explains that "the electronics controlling the storage and retrieval operations of a disk drive must have the means to precisely and reliably determine the *start of user data* in each data sector so that

---

89 USByte.com – Glossary of PC terms, 8/5/2005.

90 USByte.com – Glossary of PC terms, 8/5/2005.

data may be accurately reproduced."[91] This ***movement*** of the actuator assembly is controlled in the configuration of Malone '497, by the servo electronics and servo microcode, "which regulate a control signal to a voice coil motor."[92] Closed loop servo systems use,

> "feedback information [which is read] from the disk to find and maintain a position over a target track."[93]

As is explained by Malone '497, the:

> "feedback information may be [either] located on a signal, dedicated disk surface (*i.e.*, a dedicated servo) or embedded on data tracks between portions of data (embedded servo)."[94]

The,

> "exact composition of [primary sync] field 14 is not critical to implementation of the present invention, so long as a pattern is provided that can be distinguished in some manner by the read channel electronics of the disk drive."[95]

In other words, a primary synchronization field 14, or a secondary synchronization field has a predetermined and precise content, rather than a user dependent content, in order to form "a *pattern* that can be distinguished." As further explained by Malone '497,

> "[t]he VFO field is followed by a pattern or group of adjacent

---

91 See, by way of example of the state of synchronization in the fixed block architecture (FBA) art, Daniel J. Malone, U.S. Patent № 6.181.497 issued 30 January 2001; Daniel J. Malone, U.S. Patent № 6.124.994 issued 26 September 2000; Daniel J. Malone, U.S. Patent № 6.392.830 issued 21 May 2002; and Daniel J. Malone, U.S. Patent № 6.583.943 issued 24 June 2003, all at column 1, lines 21 through 26.

92 Malone '497, column 1, lines 44-46.

93 Malone '497, column 1, lines 46-48.

94 Malone '497, column 1, lines 48-51.

95 Malone '497, column 6, lines 4-7.

> patterns, generally referred to as 'sync bytes', that mark the beginning of the data field and provide a frame of reference for correctly distinguishing data bytes. Sync bytes are detected by sync byte detection logic in the data channel that looks for one or more predetermined sync byte patterns during a certain window of time. Once the sync byte is identified, the data bytes that follow can be properly *decoded*."[96]

As explained by one commentator,

> "[i]t is possible that the beginning of the user's data might look just like the repetitive pattern of the preamble. To precisely indicate the end of the preamble a unique, easily identify transition sequence called the ***sync mark*** or frame sync, is written in between the preamble and the user's data. The sync mark is typically 2 to 6 bytes long and may be written in two locations in case the first sync mark is missed or damaged."[97]

This conforms with the teachings of Malone '497, namely:

> "The sync byte field 14 preferably includes three adjacent bytes of sync patterns for use in a two-out-of-three voting detection scheme. It will be understood, however, that the exact composition of field 14 is not critical to implementation of the present invention, so long as a pattern is provided that can be distinguished in some manner by the read channel electronics of the disk drive."[98]

As taught by Malone '497, distinguishing a pattern "in some manner"[99] and decoding of data are two different operations; the Examining staff has however, improperly ignored these differences, and has sought without support of any evidence in the record, to equate a "sync

---

96 Malone '497, column 2, lines

97 *Action From Research*, by Action Front Data Recovery Labs, Inc., www.actionfront.com (8 August 2005).

98 Malone '497, column 6, lines 1-7.

99 Malone '497, column 6, lines 4-7.

byte" with a "data address mark."[100] It is important for the Examining staff to understand that Malone '497 does not stand alone, and that Malone '497 did not create memory storage out of whole cloth; rather, Malone '497 is simply one of the series of improvements upon the *servo sector* of disks by Steven R. Hetzler and assigned to International Business Machines.[101] Several items of the work of Hetzler, by way of example, are incorporated into Malone '497.[102] It is essential to understand the structure, nature, function and results produced by a "sync byte" as was earlier taught by Hetzler '535, and adopted by Malone '497.[103] Hetzler teaches that,

> "The function of sync byte field 26 is to tell the controller when the VCO synchronization and ENDEC flush end and the *real data*,

---

100 Paper Nos. 20051109 and 20060328define Figures 5A and 5B of Malone '497 in terms of Appellant's pending claims, substituting, for example, Appellant's "data address mark" to identify sync bytes 14, 62 of Malone '497. It has been long observed however, that if the drawings of a reference do not adequately disclose the invention defined by the pending claims, there is no anticipation. *Ex parte McIntosh*, 15 U.S.P.Q 58 (BPAI 1931).

101 *Sector Servo Data Recording Disk Having Data Regions Without Identification (ID) Fields*, by John S. Best and Steven R. Hetzler, U.S. Patent № 5.500.848 issued on the 19th of March 1996; *Fixed Block Architecture Disk File With Improved Position Identification And Error Handling*, by Steven R. Hetzler, U.S. Patent № 5.369.535 issued on the 29th of November 1994; and *Apparatus For Controlling Reading And Writing In A Disk Drive*, by Steven R. Hetzler, U.S. Patent № 5.285.327 issued on the 8th of February 1994,

102 The efforts in the art by Steven R. Hetzler, including Hetzler's concept of encoding "servo information *inside* the data sectors," are also noted in *The Elements of Design*, by Tom Thompson, BYTE.com, August 1996.

103 The *Apparatus For Controlling Reading And Writing In A Disk Drive*, by Steven R. Hetzler, U.S. Patent № 5.285.327 issued on the 8th of February 1994, is cited by Malone '497 at column 1, line 55, as teaching embedded servo disk drives. Hetzler '327 itself purports to teach improvements applicable to (*i*) CLD recording, (*ii*) banded disk using sectored servos, and (*iii*) non-sectored architecture such as count-key-data, as well as (*iv*) tape drives formated in FBA or CKD.

which is contained in field 27, *begins.*"[104]

Caution must be taken of the fact that Hetzler '327 describes a "fixed block architecture (FBA)" in which "micro *servo sectors* are *inserted in the data fields* between the conventional servo sectors to provide short bursts of *servo information*";[105] that is, sync byte field 26 in FBA is a "micro *servo sector*" which can not meet the definitions of Appellant's "data address mark recorded in ... said data field" set forth in claims 7, "data address mark regions ... recorded on said data sector" in claim 11, "writing a ... data address mark in said data block" of claim 16, "data address mark located before said servo information area in a ... data block" of claim 20, "one data block that includes ... first data address mark and a second data address mark having no servo information area therebetween" of claim 24, "a plurality of data address mark recorded on said data block at a location before said servo information area" of claim 26, "recording a data address mark ... at a ... location on a first data block preceding a servo information area" of claim 30. In short, in the art of Hetzler '535, *et sequnetia*, and Malone '497, the *sync byte* is not a part of the *real data*, but a "mciro *servo sector*" which interrupts the data block.

Turning then to the *data address mark*, rather than Malone '497's *sync byte*, as defined by the pending claims, a "data address mark" is a component not of Hetzler's and Malone '497

---

104 U.S. Patent № 5.285.327 for *Apparatus For Controlling Reading And Writing In A Disk Drive*, by Steven R. Hetzler, issued 8th of February 1994, column 3, lines 12-15. Caution must be taken of the fact that Hetzler '327 describes a "fixed block architecture (FBA)" in which "micro *servo sectors* are *inserted in the data fields* between the conventional servo sectors to provide short bursts of *servo information*. Hetzler '327, column 1, lines 34-36.

105 U.S. Patent № 5.285.327 for *Apparatus For* ..., by Steven R. Hetzler, issued 8th of February 1994, column 1, lines 34-36.

servo sector, but of a *data block*. Moreover, unlike a *sync byte*, a *data address mark*:

> "Informs [the controller] that the data is started and provides necessary synchronization when the magnetic disk driving apparatus reads the data."[106]

This means that when microcontroller 14 detects one of the two data address marks during a read operation of a sector, the possibility is avoided that the data immediately following that address mark in the corresponding data field of the data sector can not be read due to a failure to detect the data address mark. To assure that a data address mark is distinguished from other information and read, a unique pattern is used for each data address mark. By way of example, in one type of storage disk,

> "[a]n address mark is recorded in each AM field. The address mark serves to detect the boundary between blocks. This address mark indicates the recording position of the address data of a PID_n filed. The address mark includes a violation pattern violating a predetermined run length limitation. For example, the address mark includes a violation pattern ... [with a run length of 13 zeros] violates a run length limitation [*i.e.*, a RLL limitation] corresponding to run lengths of 2 to 10."[107]

In the instant application, one technique disclosed for distinguishing the data address mark is to have,

> "[t]he 7 most significant bits select any pattern defined as a user pattern ... [and] if only the 7 most significant bits are normally detected ... the micro-controller 14 skips ... and regards the

---

106 Son '387, column 4, lines 35-38.

107 *Information Recording Medium Where Address Mark Comprising Pattern Sutiable For Prevention Of Detection Error Is Recorded, And Cutting Apparatus For Reproducing The Information Recording Medium*, by Koki Tanoue, *et al.*, U.S. Patent № 6.351.448 issued on the 26th of February 2002, column 5, lines 26-34.

following information as data."[108]

As most aptly explained by Tanoue, *et al.* '448, this distinctiveness of the data address mark assuredly,

> "Prevents another pattern from being mistaken as an address mark",[109]

thereby enabling "micro-controller 14 ... [to] regard the following information as data."[110] In this manner, micro-controller 14 is both prevented from erroneously reading any other information recorded on the storage medium as a data address mark, and is thus enabled to accurately and precisely begin reading user data from the very first bit following the second data address mark.

In contradistinction, when performing its function, a "sync byte",

> "Notifies the controller that data follows".[111]

In the words of Malone '497, the "pattern or group of adjacent patterns, generally referred to as "sync bytes", that the ***mark the beginning*** of the ***data field*** and provide a frame of reference for correctly distinguishing data bytes. Sync bytes are detected by sync byte detection logic ... ."[112] A "sync byte" may be used for this purpose both prior to the servo sector data and prior to the data sector of a typical hard disk or a digital versatile disk. Within the ***data field***, the *data*

---

108 Son '387, column 6, lines 3-25.

109 Tanoue, *et al.* '488, column 5, lines 35-37.

110 Son '387, column 6, lines 3-25.

111 *Upgrading & Repairing PCs*, 8th Edition (September 1997), by Scott Mueller, MacMillan Computer Publishing, chapter 14, page 14, Table 14.5.

112 Malone '497, column 3, lines 4-8.

address mark "informs that the data ***is started.***"[113]

Given this demonstration of the differences between the actual teachings of Malone '497 and those of the misstatement of the reference asserted in the foregoing rationale given by Paper Nos. 20050510 and 20060328, there is not basis for the attempt by the Examining staff to label redundant "sync bytes" 14, 62 as Appellant's "data address bytes" because of their location in proximity to the ***data field***, because the function, characteristics and resulting affect upon micro-controller 14 are wholly different, incompatible, and are not interchangeable. Moreover, by definition, the "sync byte" of Malone '497 is not a constituent component of Appellant's "data block preceding a servo information area" as is required by, among others, claims 16 and 20. Consequently, is no anticipation of these claims under 35 U.S.C. §102(e) by the third[114] and fourth[115] embodiments of Malone '497. This rejection of claims 1 through 3, 6, 16, 17, 20, 21, 24, 26 through 28, 31, 32, 35 through 51 and 54 should not be sustained.

3. The Rejection Of Claims 1-3, 6, 16, 17, 20, 21, 24, 26-28, 31, 32, 35-51 And 54 Fails To Demonstrate Anticipation By Malone '497

Paper Nos. 20051109 and 20060328are incomplete, and it is unclear from the rationale given by the Examining staff in support of this rejection is whether the Examining staff believes that Malone '497 additionally teaches that the "Sync bytes [which] are detected by sync byte

---

113 Son '387, column 2, lines 65.

114 Shown by Figure 5A of Malone '497.

115 Shown by Figure 5B of Malone '497.

detection logic in the data channel"[116] are *decoded* as a component of the data field? Although clarification has been requested by Appellant, the Examining staff has consistently been unable pursuant to 37 CFR §1.104(a), (b) and (c) to either identify the particular teaching of Malone '497 and the corresponding referenced component of Malone '497 which teach that "sync bytes" are *decoded* as a component of the data field, or to identify pursuant to 37 CFR §1.104(a), (b) and (c) the particular teaching of Malone '497 and the corresponding referenced component of Malone '497 which teach that a "data address mark" is either "a pattern" or a "group of adjacent patterns."[117] This failure by the Examining Staff establishes on the record before the Board that there is no factual or other evidentiary basis for maintaining an assertion that Malone '497 teaches, or suggests, that a "data address mark informs the disk drive that the data is started **and** provides necessary synchronization when the magnetic disk driving apparatus reads the data."[118] Without this evidence, there is no basis for finding anticipation under 35 U.S.C. §102(e).

The sole interpretation of Malone '497 given by the Examining Staff asserts that,

> "Figures 2A, 5A-8, and 10 meet all [of] the limitations of claims 1, 16, 20, 24, 26-27, 31, 37, 40, 44, 46-47, 49, and 54. Figures 5A shows recording said data address mark to establish synchronization requested for reading user data in at least two different recording locations (14 and 62, where sync bytes correspond to the claims data address marks as they **indicate the location of the data along the track**), and Figure 8 shows when one data address mark (14) is detected (92) to establish

---

116 Malone '497, column 6, lines 4-7.

117 Malone '497, column 2, lines 62.

118 Son '387, column 4, lines 35-37.

synchronization requested for reading user data (96) ... . "[119]

A careful reading of Malone '497 establishes that Malone '497 does not support the excerpted statement of the Examining Staff made in Paper No. 20060328.

In particular, the avocation by the Examining Staff that "Figures 5A [of Malone '497] shows recording said data address mark to establish synchronization requested for reading user data in at least two different recording locations (14 and 62)" is not creditable. Malone '497 expressly teaches that,

> "the primary objective of the invention is to provide a data block format that provides a redundant sync byte field sufficiently spaced from the primary sync byte to assure readability of data despite the occurrence of disk defects spanning multiple bytes."[120]

Malone '497 continues by explaining that the,

> "precise location of the secondary fields 60 and 62 within the AGC field 10 is determined by a predetermined optimal separation 64 between primary and secondary sync bytes 14, 62."[121]

In contradistinction, it is the office of *data address marks* to:

> "informs that the data is started and provide the necessary synchronization when data is recorded or read ... . Data is the actual digital information stored in the magnetic disk."[122]

It is noteworthy that both Malone '497 and the Examining Staff place the "primary and

---

119 Paper No. 20060328, page 5.

120 Malone '497, column 7, lines 22-27.

121 Malone '497, column 7, lines 62-65.

122 Son '387, column 2, lines 65-68.

secondary sync bytes 14, 62"[123] anywhere but within the *data field* 16 [124] where a *data address mark* must be located if that *data address mark* is to function to inform "that the data is started ... ."[125] Consequently, even ignoring the structural distinctions between *sync address marks* and *data address marks*, the functional locations required for *sync address marks* physically prevents the *sync address marks* from informing "that the data is started" and for then providing "the necessary synchronization when data is recorded or read."

Turning now to the assertion by the Examining Staff that "Figure 8 shows when one data address mark (14) is detected (92) to establish synchronization requested for reading user data (96) ... ",[126] it suffices to observe that Malone '497 contradicts the Examining Staff by stating that if:

> "a sync byte 14 is detected, the timing and control circuit waits the predetermined delay period T, and then initializes and directs the transfer of a predetermined number X of data bytes from the sync byte detector 252 to the decoder 280, as shown in step **96**."[127]

In summary, Malone '497 neither teaches nor suggests either the structure, function or location of *data address marks* – Malone '497 simply does not mention *data address marks*.[128]

---

123 Malone '497, column 7, lines 62-65.

124 See Figures 1, 3, 4, 5A and 5B of Malone '497.

125 Son '387, column 4, line 35.

126 Paper No. 20060328, page 5.

127 Malone '497, column 13, lines 59-62.

128 The Examining staff seeks to dwell on superficial similarities and accidents of nomenclature between *sync address marks* and *data address marks*. By metaphor, both a *stop light* and a *stop bar* are physically placed in proximity as traffic control devices. State motor vehicle codes define *stop lights* and a *stop bars*, and on a superficial sense,

Consequently, there is no anticipation under 35 U.S.C. §102(e).

4. The Rejection Fails To Make A *Prima Facie* Showing Of Anticipation Of Claims 1-3, 6, 16, 17, 20, 21, 24, 26-28, 31, 32, 35-51 And 54 Under 35 U.S.C. §102(e)

Malone '497 teaches that,

> "[t]he VFO field is followed by a pattern or group of adjacent patterns, generally referred to as 'sync bytes', that mark the beginning of the data field and provide a frame of reference for correctly distinguishing data bytes. Sync bytes are detected by sync byte detection logic in the data channel that looks for one or more predetermined sync byte patterns during a certain window of time. Once the sync byte is identified, the data bytes that follow can be properly *decoded*"[129],

and the sync byte is distinguished "in some manner by the read channel electronics of the disk drive"[130], while the data which has been written in the data field is decoded. In contradistinction to the "sync byte" of Malone '497, the "data field" is user supplied, and inherently lacks a particular composition or pattern.

The "data address mark informs the disk drive that the data is started and provides necessary synchronization when the magnetic disk driving apparatus reads the data."[131]

---

both are in close proximity to one another and both direct a motorist where to stop a motor vehicle. In a more literal sense, only a *stop light* instructs a motorist *when* to stop and only a *stop bar* instructs the motorist about the precise and exact location *where* that stop, which is being required by the *stop light*, must be completed. In the same sense, only a *data address mark* "informs that the data is started" (*i.e.*, that the signal which is being currently detected is user data).

129 Malone '497, column 2, lines

130 Malone '497, column 6, lines 4-7.

131 Son '387, column 4, lines 35-37.

Another commentator teaches that,

> "[a]n address mark functions advantageously to achieve byte (a set of eight binary bits) synchronization. In particular, an address mark serves for identifying a sector header or the leading edge of a stream of used [*sic*, "user"] data bits. ... Preferably, each address mark within a given sector 25 is defined by a unique pattern of signal transitions to readily distinguish the address marks from each other within a sector and from the rest of the bit stream."[132]

Inherent in a "data address mark" is an "address at the beginning of ... the data field of the track format."[133] Moreover, Appellant's "data address mark" is a constituent component of a "data field."[134] Inherent in a "data address mark" is an "address at the beginning of ... the data field of the track format";[135] an "address" aspect is not a characteristic of a "sync byte" and Malone '497 nowhere suggests that his "primary and secondary sync bytes" exhibit any characteristic of a "data address mark."

Specifically, Malone '497 teaches a "primary sync field 14" and a "secondary sync field 62" that are patterns which "can be distinguished in some manner by the read channel electronics of the disk drive"[136] while Appellant's claims define "data address marks" that are

---

132 *Windowing Method Of And Apparatus For Address Mark Detection*, by Kenneth E. Herting, U.S. Patent № 5.047.877 issued on 10th of September 1991, column 1, lines 34-40 and column 3, lines 64-67. Cited by the Examiner in Paper Nos. 20050510 and 20060328.

133 USByte.com – Glossary of PC terms, 8/5/2005.

134 Son, U.S. Patent № 5.963.387 issued 5 October 1999, column 4, lines 26 and 27.

135 USByte.com – Glossary of PC terms, 8/5/2005.

136 Malone '497, column 6, lines 6 and 7.

address specific relative to other address marks within a sector.[137] Unlike the "data address mark" of the pending claims which serves "to readily distinguish the address marks for each other within a sector and from the rest of the bit stream",[138] the "sync byte field 14, 62" of Malone '497 is simply "a pattern".[139] Although "the 'sync bytes'" may accurately, as taught by Malone '497 "mark the beginning of the data field and provide a frame of reference for correctly distinguishing data bytes", those "sync byte fields 14, 62" fail to provide an address mark for each of the data fields. The inability of "primary sync field 14" and "secondary sync field 62" to serve as a data address mark for a data field negates any possibility of anticipation under 35 U.S.C. §102(e). Withdrawal of this rejection is therefore required.

5. The Rejection Fails To Consider *The Invention* As Defined By Claims 1-3, 6, 16, 17, 20, 21, 24, 26-28, 31, 32, 35-51 And 54 As Required Under 35 U.S.C. §102(e)

35 U.S.C. §102(e) requires that an Appellant be issued a patent, *unless* "(c) the invention was described in ... a patent granted on an application for patent by another filed in the United States before the invention by the Appellant ... ." That bar to issue of Appellant's reissue patent has not been met.

Malone '497 teaches that,

---

137 See, for example, Herting, U.S. Patent № 5.047.877, *supra*, column 3, lines 65-67.

138 Herting, U.S. Patent № 5.047.877, *supra*, column 3, lines 65-67.

139 Malone '497, column 6, lines 4-7. "It will be understood, however, that the exact composition of field 14 is not critical to implementation of the present invention, so long as a pattern is provided that can be distinguished in some manner by the read channel electronics of the disk drive."

> "[t]he VFO field is followed by a pattern or group of adjacent patterns, generally referred to as 'sync bytes', that mark the beginning of the data field and provide a frame of reference for correctly distinguishing data bytes. Sync bytes are detected by sync byte detection logic in the data channel that looks for one or more predetermined sync byte patterns during a certain window of time. Once the sync byte is identified, the data bytes that follow can be properly *decoded*"[140],

and the sync byte is distinguished "in some manner by the read channel electronics of the disk drive"[141], while the data which has been written in the data field is decoded. Singularly absent from Malone '497 is any teaching or suggestion of how to make patterns which "can be distinguished in some manner by the read channel electronics of the disk drive" concomitantly sequentially different in consecutive variety to serve as specific addresses of data fields. Nowhere does Malone '497 endow either of his "primary sync field 14" or his "secondary sync field 62" with an office of providing an address of one of a plurality of "data fields." These "sync bytes" identify no address. From another perspective, Malone '497 teaches that his "synch byte fields 14, 62" are each multiple byte patterns,[142] while each of Appellant's ""data address marks" are, in essence, the "7 most significant bits of ... a data address mark constructed by 8 bits ... ." [143] In substance, the Examining staff has improperly ignored the characteristics of

---

140 Malone '497, column 2, lines

141 Malone '497, column 6, lines 4-7.

142 See once again, Malone '497, column 6, lines 3-7, "It will be understood that the exact composition of field 14 is not critical ... so long as a pattern is provided that can be distinguished in some manner ... ."

143 Son '387, column 6, lines 20-22, which read: "For example, if only the 7 most significant bits are normally detected at the same time of detecting a data address mark constructed by 8 bits, ..."

Appellant's "data address" feature of "the invention"[144] defined by each of the pending claims, and without basis in the record, sought to summarily equate Appellant's "data address marks" with the "primary 14" and "secondary sync byte 62" of Malone '497. Absent teaching or suggestion of every aspect of a claim within a single reference, there is no anticipation and this rejection may not be sustained.

E. Rejection of Claims 7-15 Under 35 U.S.C. §103(a)

Claims 7 through 15 are again rejected under 35 U.S.C. §103(a) as being unpatentable over the proposed combination of what the Examining staff endeavors to label the "Admitted Prior Art" and Malone Sr. '497. Appellant respectfully traverses this rejection for the following reasons.

1. The Rejection Of Claims 7 Through 15 Under 35 U.S.C. §103(a) Depends Upon A Technically Inaccurate Interpretation Of The Examiner's Proposed Combination Of Art.

In support of this rejection, Paper Nos. 20051109 and 20060328 states that,

> "Malone, Sr. Figure 5A shows recording a data address mark to establish synchronization requested for reading user data in at least two different recording locations (14 and 62, where sync bytes correspond to the claimed data address marks as the indicate the location of the data along the track) ... ."[145]

As noted earlier here, the Examiner's proposed combination incorporating Malone '497 nowhere uses the phrase "data address mark", and identifies reference locations 14, 62 as "primary sync

---

144 35 U.S.C. §102(e). "A person shall be entitled to a patent unless ... (e) the *invention* was described in ... (2) a patent granted on an application for patent by another filed in the United States before the invention by the Appellant for patent ... ."

145 Paper Nos. 20050510 and 20060328, Examiner's comments, page 4.

byte field 14"[146] and "secondary sync byte field 62."[147] Consequently, the assertion of the Examining staff that in the Examiner's proposed combination incorporating "Malone, Sr. Figure 5A shows recording a data address mark to establish synchronization requested for reading user data in at least two different recording locations (14 and 62," is fiction, wholly unsupported by the record. Withdrawal of this rejection is therefore required.

2. The Rejection Of Claims 7 Through 15 Under 35 U.S.C. §103(a) Fails To Make A *Prima Facie* Showing Of Obviousness.

In support of this rejection, Paper Nos. 20051109 and 20060328 states that,

> "Malone, Sr. ... Figures 8 and 10 show detecting said data address mark to confirm validity of user data following said data address mark (92, 94) ... ."[148]

As noted earlier here, the Examiner's proposed combination incorporating Malone '497 nowhere uses the phrase "data address mark",[149] and in his explanation of Figures 8 and 10, describes step 92 as "a primary sync byte detection step 92"[150] in which,

> "Sync byte detector 252 searches for at least two out of three primary sync byte patterns for the duration of the sync detection

---

146 Malone '497, column 12, line 65.

147 Malone '497, column 14, line 6.

148 Paper Nos. 20050510 and 20060328, Examiner's comments, page 4.

149 A more technically accurate reading of the Examiner's proposed combination incorporates two "sync byte fields 14, 62" and employs those synch byte field for the same purpose, and with the same results as are taught by Malone '497.

150 Malone '497, column 13, line 40.

timing window previously described."[151]

Claims 7 and 11 however, define,

> "recording a data address mark, during a recording mode, in at least two different locations of said data field immediately preceding a data area containing user data;
> detecting said data address mark recorded in said different locations of said data field, during a reading mode, to confirm validity of user data contained in said data area following said data address mark;"

and,

> "at least two different data address mark regions for use to indicate a validity of data recorded on said data sector is written ... ."

Ignoring *arguendo* the complete absence of any teaching or suggestion in the Examiner's proposed combination about Appellant's use of more than a single "data address mark", that proposed combination is utterly devoid of teaching about Appellant's employment of "different data address mark regions for use to indicate a validity of data recorded on said data sector"[152] or "to confirm validity of user data contained in said data area following said data address mark."[153] Consequently, Paper Nos. 20051109 and 20060328fail to make a *prima facie* showing of obviousness under 35 U.S.C. §103(a).

3. The Rejection Of Claims 7 Through 15 Under 35 U.S.C. §103(a) Is Impermissibly Based Upon A Fatally Flawed Understanding Of The Examiner's Proposed Combination Of Art.

---

151 Malone '497, column 13, lines 41-43.

152 Pending claim 11.

153 Pending claim 7.

Returning to the rationale given in Paper Nos. 20051109 and 20060328 for this rejection, namely the assertion of the Examining staff that,

> "Malone, Sr. ... Figures 8 and 10 show detecting said data address mark to confirm validity of user data following said data address mark (92, 94) ...",[154]

and the contradiction of this assertion made by the express contrary statement taken from the Examiner's proposed combination incorporating Malone '497, which describes step 92 as "a primary sync byte detection step 92"[155] in which,

> "Sync byte detector 252 searches for at least two out of three primary sync byte patterns for the duration of the sync detection timing window previously described."[156]

Paper Nos. 20051109 and 20060328however, assert that its proposed combination skips "a remaining mark (62) when any ***one mark*** is normally detected (98)," an assertion that is at variance with the express teachings of the Examiner's proposed combination.

Moreover, claims 7 and 11, define,

> "skipping a remaining data address mark recorded in said different recording locations of said data track, when said data address mark recorded in said at least one of said different recording locations is detected",

and,

> "said transducer head not utilizing a remaining data address mark recorded in said different recording locations of said data track, when a data address mark recorded in said two different data address regions is detected,"

---

154 Paper Nos. 20050510 and 20060328, Examiner's comments, page 4.

155 Malone '497, column 13, line 40.

156 Malone '497, column 13, lines 41-43.

which is not the same feature, and is not preformed in the same manner, and does not produce the same result as the Examiner's proposed combination's technique of using "sync byte detector 252" to search "for at least two out of three primary sync byte patterns for the duration of the sync detection timing window previously described."[157] Ignoring *arguendo* the fact forgotten by Paper Nos. 20051109 and 20060328that the "sync byte field" lacks a "data address" aspect, were in the record of this prosecution is the evidence of the motivation in either the primary reference or in the secondary reference for replacing a primary sync byte field 14 and a secondary sync byte field 62 with Appellant's "data address mark"[158] which may advantageously employed to inform "the disk drive that the data is started and provides necessary synchronization when the magnetic disk driving apparatus reads the data"?[159] Given the absence of such evidence, a fair reading of the Examiner's proposed combination is the very same use of "sync byte detector 252" searching "for at least **two out of three primary sync byte patterns** for the duration of the sync detection timing window previously described,"[160] as opposed to Appellant's:

---

157 Malone '497, column 13, lines 41-43.

158 The sole evidence of motivation advocated by Paper Nos. 20050510 and 20060328, page 5, is "to provide sync byte redundance to improve overall disk drive reliability in a headerless servo recording system." This assertion is meaningless as evidence of the requisite evidence of motivation necessary to make a *prima facie* showing of obviousness; in essence, this assertion is **primarily** an admission that the Examiner's proposed combination fails to make a *prima facie* showing of obviousness of claims 7 through 15 with Appellant's "data address mark recorded in said different locations of said data field", and **secondarily** an admission by the Examining staff that the Examiner's proposed combination fails to endow the data field with the attributes of an address mark.

159 Son '387, column 4, lines 35-37.

160 Malone '497, column 13, lines 41-43.

> "skipping a remaining data address mark ... when said data address mark ... is detected",

and,

> "not utilizing a remaining data address mark ... when a data address mark ... is detected."

The contrast between Appellant's singular and the plural number of the Examiner's proposed combination is itself convincing *indicia* of the non-obviousness of claims 7 through 15.

Furthermore, "data address marks" are not customarily read and decoded during a "sync detection timing window"; there is simply no evidence in the record created by the examining staff to support reading and decoding of a data address mark during the "sync detection timing window" as is required by the Examiner's proposed combination. Absent this evidence, this rejection may not be maintained.

A more technically accurate reading of the Examiner's proposed combination would incorporate the two "sync byte fields 14, 62" and employ those synch byte fields for the same purpose, and with the same results as are taught by Malone '497, without consideration of either the structural inability of a disk drive as defined by claims 11 through 15, or a method for forming and processing a data sector as defined by claims 7 through 10, could be reliably employed within the extremely short interval of "seek time" allotted, to "inform that the data is started and provide necessary synchronization when the magnetic disk driving apparatus reads the data."[161] Moreover, the advantage attainable with the practice of claims 7 and 11 is unavailable with the Examiner's proposed modification of the primary reference simply because

---

[161] Son '387, column 4, lines 35-37.

incorporation of the two "sync byte fields 14, 62" taught by Malone '497 and employment of those synch byte fields necessarily restricts the combination of the Examining Staff to the same results as are taught by Malone '497, simply because, for among other deficiencies, the two "sync byte fields 14, 62" taught by Malone '497 physically can not serve to "informs that the data is started and provides the necessary synchronization"[162] as taught by Appellant. In short, neither Appellant's improvement in the resulting seek and read reliability are attained with the Examining Staff's proposed modification, nor are the resulting structural or operational modifications of the art made by Appellant; simply put, two "synch byte fields" are not fungible or interchangeable. Accordingly, absent either Appellant's structure, operational mode and advantageous results, and absent evidence in the record of the motivation for modifying the primary reference in the manner required by the Examiner's proposed combination, this rejection may not be sustained. Such action is respectfully urged.

F. Rejection of claims 16-54 Under 35 U.S.C. §251

Claims 16 through 54 are finally rejected under 35 U.S.C. §251 as being improper recapture of broadened claimed subject matter surrendered in the application for the patent upon which the present reissue is based. The Examiner contends that a broadening aspect, which was not present in the application for patent, is present in the reissue application, and that the broadening aspect in the reissue application relates to the subject matter which Appellant previously surrendered during the prosecution of the application. Appellant again respectfully

---

[162] Son '387, column 4, lines 35-38.

traverses this rejection for the following reasons.

In support of this rejection, Paper Nos. 20051109 and 20060328 assert that,

> "[t]he record of the application for the patent shows that the broadening aspect (in the reissue) relates to subject matter that Appellant previously surrendered during the prosecution of the application. ... claims 16, 20, 24, 26, 31, and 35-54 ... omitted the language *skipping a remaining data address in said different recording locations of said data track, when any one data address mark recorded in said different recording locations is normally detected* and *said transducer head not utilizing a remaining data address mark recorded in said different recording locations of said data track, when a data address mark recorded in a different data address regions is detected.* This language was specifically added to claim in the original patent place it in condition for allowance.[163]

This rationale provides no justification on the instant record to maintain this rejection.

1. Paper Nos. 20051109 and 20060328Improperly Impose A *Per Se* Rule Of Reissue Recapture To Justify A Rejection Of Claims 16-54 Under 35 U.S.C. §251

The Examining staff has improperly sought to impose a *per se* rule of reissue recapture to prevent Appellant from retreating from any claim limitation determined to have secured allowance of the original patent

In essence, the Examining staff is arguing that because claims were amended prior to allowance of the parent patent, no claim may be granted in a reissue application which does not contain either of the two limitations incorporated into the patent's claims. This is a *per se* rule of reissue recapture. Nothing in 35 U.S.C. §251 supports this *per se* rule of reissue recapture; moreover, the practice in the U.S. Patent & Trademark Office does not support this *per se* rule.

The first clause cited in Paper Nos. 20050510 and 20060328, *skipping a remaining data*

---

[163] Paper Nos. 20050510 and 20060328, page 6.

address in said different recording locations of said data track, when any one data address mark recorded in said different recording locations is normally detected,[164] was initially set forth in original dependent claim 2, and in an amendment of parent patent claim 1 made on the 29th of March 1999, was added to claim 1 (now patent claim 1). The Examining staff had determined that dependent claim 2 was allowable if rewritten in independent form. The second clause, *said transducer head not utilizing a remaining data address mark recorded in said different recording locations of said data track, when a data address mark recorded in a different data address regions is detected,*[165] was initially set forth in original dependent claim 13, and in an amendment of parent patent claim 11 also made on the 29th of March 1999, was added to claim 11 (now patent claim 11). Claim 13 had also been determined by the Examining staff to be allowable.

As was carefully explained by the Board of Patent Appeals and Interferences on the *Request for Rehearing* in *Ex parte Eggert*, Appeal № 2001-0790 decided on the 29th of May 2003, [166]

> "The changing scope of a claim during the administrative examination process as it is amended to overcome prior art rejections can be viewed as a series of concentric circles."

---

164 Although not identified by Paper Nos. 20050510 and 20060328, this clause is taken from the amendment of independent process claim 1 made on the 29th of March 1999.

165 Although not identified by Paper Nos. 20050510 and 20060328, this clause is taken from the amendment of independent apparatus claim 11 made on the 29th of March 1999.

166 *Ex parte Eggert*, et al., 67 USPQ2d 1716 (BAPI; 2003); cited by the *Manual of Patent Examining Procedure*, 8th Ed, Rev. 2, §§ 716.02 and 1412.02.

This reasoning by the Board may not be ignored by the Group Art Unit. Succinctly, the outer concentric circle mentioned by the Board represents, in the opinion of the Board, the scope of coverage of the unamended claims in the parent application that were subject to rejection during prosecution of the patent, while the inner concentric circle represents the scope of the amended, and issued patent claims. In the view of the Board, the surrendered subject matter is the outermost of the concentric circles. The subject matter between the concentric circles however,

> "was not subject to the administrative examination process as the examiner was never directly presented with a claim which fell within the scope of coverage which exists between the inner and outer concentric circles."

Thus, the Board determined that,

> "appellants have never conceded that a claim falling within the scope of the"

area **between** the concentric circles,

> "is unpatentable and therefore, in our view, such subject matter is not barred by the recapture rule."

On the basis of this evidence, the Board explained that the approach of the Examining staff was to argue for a *per se* rule, and the Board both refused the approach of the Examining staff and refused to sustain the reissue recapture rejection.

In the instant matter, the scope of the pending claims falls within the area between the inner and outer concentric circles, that is, between the scope of the originally presented claims and the scope of the amended patent claims, and are not the subject of any disclaimer by Appellant. Nowhere in the record is there any evidence supporting the Examiner's assertion that

the act of amending an allowable claim in the parent patent is an act of estoppel. Moreover, the record before the Examiner establishes that the parent patent was the subject of but a single amendment, and that Appellant made no disclaimer on the record. There is therefore, no basis for maintaining this rejection. Its withdrawal is required.

2. Paper Nos. 20051109 and 20060328 Provide No Justification For A Rejection Of Claims 16-54 Under 35 U.S.C. §251

As noted in the foregoing paragraphs, no effort has be made in Paper Nos. 20051109 and 20060328 to demonstrate a disclaimer by the Appellant of the patentability of the subject matter defined by claims 16 through 54. The Examining staff has incorrectly applied the rule of reissue recapture in a manner that is contrary to the language of 35 U.S.C. §251, which expressly contemplates reissue of broader claims.[167] Consequently, on this record, there is no evidence to support a finding of "reissue recapture" because nowhere in the record has Appellant stated that either the first clause, *skipping a remaining data address in said different recording locations of said data track, when any one data address mark recorded in said different recording locations is normally detected,*[168] or the second clause, *said transducer head not utilizing a remaining data address mark recorded in said different recording locations of said data track,*

---

167 35 U.S.C. §251 carefully defines the circumstances under which an enlargement "of the scope of the claims of the original patent" may not be granted. The evidence before the Examining staff provides no basis under 35 U.S.C. §251 for refusing Appellant's application for an enlargement of the scope of the claims of the original patent.

168 Although not identified by Paper Nos. 20050510 and 20060328, this clause is taken from the amendment of independent process claim 1 made on the 29th of March 1999.

when a data address mark recorded in a different data address regions is detected,[169] constituted the an outer boundary upon the scope of coverage of Appellant's inventions. Moreover, the record before the Examiner establishes that the parent patent was the subject of but a single amendment, and that Appellant made no disclaimer on the record. Absent a basis established by the evidence of record, this rejection must be withdrawn. Such action is respectfully solicited.

3. **The Final Rejection Of Claims 16-54 Under 35 U.S.C. §251 Is Substantively Inadequate Because Paper Nos. 20051109 and 20060328 Fail To Address Appellant's Response To The Rejection Of Claims 16-54 Made In Papers Nos. 13 and 19, In Response To Office Actions Issued On 24 November 2004 And 18 May 2005**

First, in Paper № 13, the Examiner asserted that,

> "[a] broadening aspect is present in the reissue, which was not present in the application for patent. The record of the application for the patent shows that the broadening aspect (in the reissue) relates to subject matter that Appellant previously surrendered during the prosecution of the application. Accordingly, the narrow scope of the claims in the patent was not an error within the meaning of 35 U.S.C. §251, and the broader scope surrendered in the application for the patent cannot be recaptured by the filing of the present reissue application."

The Examiner's assertion is an incorrect application of 35 U.S.C. §251, that raises several issues. Examination of these issues reveals an absence of justification for the Examiner's application of 35 U.S.C. §251 to support this rejection.

Second, in the application of 35 U.S.C. §251 to support this rejection of Appellant's reissue claims 16-51, the Examiner has argued that:

---

[169] Although not identified by Paper Nos. 20050510 and 20060328, this clause is taken from the amendment of independent apparatus claim 11 made on the 29th of March 1999.

> "In claims 16-51, Appellant has omitted the language '*skipping a remaining data address in said different recording locations of said data track, when any one data address mark recorded in said different recording locations is normally detected*' and '*said transducer head not utilizing a remaining data address mark recorded in said different recording locations of said data track, when a data address mark recorded in a different data address regions is detected*'. This language specifically added to claims in the original patent to place it in condition for allowance".

The Examiner's assertion is improper as a matter of law. The Examiner's attention is invited to the rejection, which is based upon the statute set forth in 35 U.S.C. §251, which provides that:

> "Whenever any patent is, through error without any deceptive intention, deemed wholly or partly inoperative or invalid, by reason of ... the patentee claiming more or less than he had a right to claim in the patent, the Director shall ... reissue the patent for the invention disclosed in the original patent, and in accordance with a new and amended application ... ."

Moreover, 35 U.S.C. §251 expressly contemplates issuing a reissue patent with claims that are broader than those issued in the patent. Specifically, 35 U.S.C. §251 states that:

> "No reissued patent shall be granted enlarging the scope of the claims of the original patent unless applied for within two years from the grant of the original patent"

The instant application was in fact filed within the two year window.

In the Examiner's response and argument, the Examiner argues that the Appellant's statement that "forming and processing a data address mark" defers from "a method of providing a data block", describing the step of "writing" rather than "the step of processing in address mark" is, in the Examiner's opinion, erroneous. The basis for the Examiner's disagreement is the Examiner's assertion that the phrase taken from the preamble of independent, rejected claim

16, namely "a method of providing a data block" encompasses the "processing step" defined by dependent claims 18 and 19. The Examiner is cautioned that the rejection and the examination should be of independent claim 16; any effort by the Examiner to read features from dependent claims 18 and 19 into independent claim 16, is unauthorized and impermissible. Claim 16 is an independent claim; moreover, claim 16 was presented in this application to provide a broader scope of coverage than was found in the claims of the Appellant's U.S. Patent № 5,963,387. The fact that the scope of coverage provided by claim 16 is broader in scope, is no basis for a reissue capture rejection under 35 U.S.C. §251. Furthermore, the presence of dependent claims such as 18 and 19 which define other and additional steps of "processing' provides no basis in U.S. practice for interpreting a single preamble phrase of a patent claim. The impropriety of the Examiner's argument demonstrates is fallaciousness.

The Examiner continues to argue that the verb "providing" encompasses both "the writing as well as [the] forming and processing." It is unclear why the Examiner has made this assertion, because the verb "providing" is a single verb found in the preamble of claim 16. Any question of reissue recapture under 35 U.S.C. §251 is determined by prosecution of the patent application, rather than misguided efforts by the Examiner to improperly read into an independent claim, features defined by claims depending upon that independent claim.

The Examiner continues in this vein by persisting in an effort to limit the scope of coverage provided by independent claim 26, based upon the Examiner's endeavor to read features defined by dependent claims 27, 29 and 30 into independent claim 26. Claim 26 stands upon its own, and its scope of coverage is interpreted broadly, unlimited by the language of

claims depending upon independent claim 26. Moreover, claim 26 expressly defines a "method for reading a data block." Consequently, whether "reading" or "writing" may be characterized as "processing", the fact is the Examiner's interpretation of single verbs in independent claims 16 and 26 is pointless and unmerited by the prosecution history of this application. Attempts to limit the scope of coverage accorded to theses independent claims by improperly attributing features found in their dependent claims, is contrary to statute. Questions of reissue recapture simply may not be resolved by resorting to the language of the dependent claims. Withdrawal of the line of reasoning in subsequent Office correspondence is respectfully requested.

Third, the Examiner's interpretation of claims 16 through 51 in a misguided effort to justify reissue recapture is, as was previously explained to the Examiner, is incorrect on the facts presented by the prosecution history. The Examiner's attention is again invited to consider the two features of claims 1-15 quoted by the Examiner described the method steps accompanying the "processing [of] a data address mark" as defined by method claims 1 and 7, and there accompanying dependent claims 2-6 and 8-10, and the operation of the transducer head assembly 6 as controlled by microcontroller 14, as is expressly defined by apparatus claim 11, together with its dependent claims 12-15. In contradistinction, Appellant's rejected claims 16-51 define different aspects and features of Appellant's invention, with apparatus claims directed to either the recording medium as defined by claims 20-23, 38, 39 or 40, or directed to the disk drive device as defined by claims 24, 25, 32-34, 41, 42, 43, 50, 51 and newly presented reissue claim 52. The two features of method claims 1 and 7 cited by the Examiner of "skipping a remaining data address" and the functional operational feature of claim 11 with "said transducer

head not utilizing a remaining data address mark" cited by the Examiner have nothing to do with Appellant's reissue claims directed to either the recording medium or to the disk drive device itself. Either feature of "skipping a remaining address" or "said transducer head not utilizing a remaining data address mark" could not lawfully be incorporated into Appellant's apparatus claims directed to either the recording medium or the disk drive device, without creating an aggregation impermissible under the second paragraph of 35 U.S.C. §112. In short, the subject matter of method claims 1 and 7 and apparatus claim 11 of either "skipping a remaining data address" or "not utilizing a remaining data address mark" are not aspects of Appellant's reissue claims directed to the recording medium or of Appellant's reissue claims defining the disk drive device..

Turning to the reissue method claims, Appellant has presented three general categories of processes: one, a method of providing a data block defined by claims 16-19 and 35-37, and newly presented independent claims 53 and 54; two, a method of reading a data block defined by claims 26-30, 44, 45 and 46; and three, a method of preparing a memory disk defined by independent claims 31 and 47. The features of amended patent method claims 1 and 7 define "forming and processing a data address mark", while Appellant's first group of reissue process claims 16-19 and 35-37, which define a method of providing a data block, describe the step of "writing", rather than the step of "processing a data address mark" as defined by amended patent claims 1 and 7. The second group of reissue method claims 26-30, 44, 45 and 46 define a method of reading a data block, as opposed to "processing a data address mark" as defined by amended patent process claims 1 and 7 cited by the Examiner. Appellant's third group of reissue

process claims, namely independent process claims 31 and 47 describe a method of preparing memory disk with one or more recording steps, as opposed to the "processing a data address mark" defined by amended patent process claims 1 and 7 cited by the Examiner.

In summary, Appellant's reissue claims are directed to different apparatus and to different methods than those defined by independent amended patent process claims 1 and 7, or independent amended disk drive apparatus claim 11. Consequently, recapture of any subject matter surrendered by the amendment of patent claims 1, 7 and 11 is not an issue here--the subject matter of the patent claims is wholly different from the subject matter of the apparatus and method reissue claims 16-54 now pending.

Fourth, the Examiner supports this rejection under 35 U.S.C. §251 by asserting that the amendment of claims 1, 7 and 11 in Appellant's patent surrendered "the broader scope" in "the application for patent", and that the broader scope "cannot be recaptured by the filing of the present reissue application." The Examiner relies upon decisions such as *Pannu v. Storz*, 258 F.3d 1366 (Fed. Cir. 2001) and *Hester Industries, Inc. v. Stein, Inc.*, 46 USP2d 1641 (Fed. Cir. 1998) to buttress the Examiner's assertion. In Paper № 5 issued on the 30th of December 1998, the Examiner rejected claims 1, 7, 11 and 12 under 35 U.S.C. §102(b) as anticipated by Geld '545. Subsequently, in Appellant's responsive amendment filed on the 29th day of March 1999, Appellant "amended the independent claims 1, 7, and 11 to incorporate feature of allowable claims 2, 8, and 13, respectively." Additionally, Appellant expressly noted that there was no anticipation under 35 U.S.C. §102(b) "unless all of the elements of a claim are found in exactly the same situation and united in the same way in a single prior art reference, and thus every

element must be literally present and must also be arranged as in the claim", (see Paper № 6, Pg. 8, and then explain that the Examiner "appears to be misapplying the facts to Gold '545 here" because "the first address mark (AM) is included within the ID header 22 and is not considered to be a *data* address mark" while the "second address mark (AM) is included within the *data* header 24 is considered to be a *data* address mark." Appellant concluded the explanation of a lack of anticipation by explaining to the Examiner that "Gold '545 does not teach or suggest a recording of a data address mark in two locations, as set forth in Appellant's independent claims 1, 7, and 11." Appellant's remarks, amendment of 29 March 1998, pg. 8. In summary, Appellant made no surrender, identified the impropriety of the Examiner's anticipation rejection and in compliance with 37 CFR §1.111(a) and (b), pointed out the specific distinctions that rendered those claims patentable over Gold '545. The fact that Appellant identified the Examiner's misapplication of the facts of Gold '545 does not constitute surrender of either the scope or breadth of the subject matter defined by claims 1, 7 and 11. Appellant presented no argument in the demonstration of the Examiner's misapplication of Gold '545 that the amendment itself patentably distinguished any of the amended claims over Gold '545. Appellant instead presented a factual basis for the impropriety of the anticipation rejection of those claims based upon the language of claims 1, 7 and 11 as rejected. Consequently, there was neither argument nor amendment to narrow the scope of claims 1, 7 and 11 in order to overcome the prior art. Absent argument and amendment to overcome the prior art, there is no surrender. Amendment of claims 1, 7 and 11 for reason other than an effort to overcome the prior art is irrelevant in applying the doctrine of reissue recapture.

Specifically, in Paper № 6 Appellant explained that although the Examiner had argued in Paper № 5 that U.S. Patent № 5,231,545 issued to Gold (hereinafter Gold '545) "teaches recording a data address mark in at least two different locations of the data track (fig. 1A)," the Examiner appeared to be misapplying the facts of Gold '545 because in Figure 1A of Gold '545, the first address mark (AM) is included within the *ID* header 22 and is not considered to be a "data" address mark. The second address mark (AM) is included within the *data* header 24 and is considered to be a "data" address mark. In conclusion, Gold '545 does not teach or suggest a recording of a data address mark in two locations, as set forth in the Appellant's independent claims 1, 7, and 11.

There is no anticipation under 35 U.S.C. §102 unless all of the elements in a claim are found in exactly the same situation and united in the same way in a single prior art reference, and thus every element must be literally present and must also be arranged as in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (CAFC 1989). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970), and the Manual of Patent Examining Procedure (M.P.E.P.) 2143.03. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Therefore, absence from the reference of any claimed element negates anticipation. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 230 USPQ2d 81 (Fed. Cir. 1986). See also M.P.E.P. 2131 and 35 U.S.C. §102.

To establish a *prima facie* case of obviousness, three basic criteria must be met. **First,** there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. **Second,** there must be a reasonable expectation of success. **Third,** the prior art reference (or references when combined) must teach or suggest all the claim limitations. See the *Manual of Patent Examining Procedure* (M.P.E.P.) §2143 and 35 U.S.C. 103. If the Examiner fails to establish a *prima facie* case, the rejection is improper and will be overturned. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Gold '545 does not set forth the each and every element of the claims 1, 7, and 11, as amended. Thus, Gold '545 does not anticipate the Appellant's claims, as amended, and therefore Gold '545 does not support a rejection of claims under 35 U.S.C. 102. In addition, Gold '545 does not teach or suggest the features set forth in Appellant's claims, such as the two *data* address marks and the skipping of one data address mark. Thus, Gold '545 does not support a rejection of claims under 35 U.S.C. 103. The additional cited prior art does not remedy the deficiencies of Gold '545. That is, Hirukawa '693, Otsuki '207, and Yamawaki '745 in combination with Gold '545 do not teach or suggest the aforementioned features of the Appellant's claims, and thus do not support a rejection of claims under 35 U.S.C. §103. Consequently, absent surrender, the condition precedent to invocation of the doctrine of reissue recapture does not exist; withdrawal of this rejection is therefore required.

CONCLUSION

First Paragraph of 35 U.S.C. §112

On the twin issues of enablement, namely a written description and a teaching of how to make and use Appellants ... regulating, it suffices to observe that in is recognized in the art that the disk drive continuously regulates movement of the heads and the disk; it is the successful identification of an address (reading or writing), or the inability to reliability identify an address (to read or to write), which is the impetus for continued regulation and continued movement of the head and disk (in order to either proceed to the next address or to endeavor in a second, or higher repetition to locate the current address) that is precisely what such exemplars of the art as Malone '497 teaches when he is unable to read his *primary sync bytes*. Specifically, Malone '497 teaches that "[a]ccording to this first embodiment, if a primary sync byte field is unreadable, an error recovery procedure is invoked and the channel **attempts a read** of the secondary sync bytes ***on a subsequent revolution***."[170] Art such as the IBM series of references of record continue to regulate movement of the heads in efforts to read during subsequent revolutions of the head; Appellant continues during the practice of the inventions defined by claims 32 through 34 and 50 through 52, with regulation of movement of the head to based on one of the first or second data address marks by, for example, regulating movement of the head to proceed to the next address when a successful reading of the first data address mark at the current address is indicated (which concomitantly indicates that the signal read immediately subsequent to the first and second data address marks is user data), without the necessity of

[170] Amendment filed by Malone '497 on the 25th of January 1999, page 2. A copy has been entered in the record.

regulating movement of the head to make repetitious efforts to identify a current address on the disk during multiple revolutions of the disk as is taught by Malone '497. In short, any control of the activity of the head for any purpose described in the application satisfies both the *written description* clause and the *enablement* clause of 35 U.S.C. §112. Here, the Examining staff seems to have wholly ignored the fact that in the hard disk drive art, (*i*) any successful step of reading either a first address mark or a second address mark is inevitably followed by the necessity of "regulating movement of the head" in the process of proceeding to the next address, simply because one of Appellant's first and second data address marks indicates that the immediately following signal is user data and the step of regulating movement of the head must be effected to immediately follow Appellant's first and second data address marks in order to compensate for the fact that storage of user data on a hard disk is fragmented. Moreover, (*ii*) a failure to read one of Appellant's first and second data address marks also necessitates "regulating movement of the head" in a compensatory scheme such as continuing the endeavor to read one of Appellant's first and second data address marks for example, during a subsequent revolution of the disk. In either scenario, as well as in other operations, a disk drive device as taught by Appellant's specification must have a controller constructed to base its regulation of the head on at least one of the data address marks as is defined by claims 32, 50, 51 and 52. The fact that one of Appellant's data address marks has been either read or not read, provides no factual basis for the Examining staff to rule that no step of "regulating movement of said head" is taught as subsequently occurring, or that an subsequent step of "regulating movement of said head" excludes considerations by the controller of operational parameters other than Appellant's

first and second data address marks.

Disk drives are "always running", that is, always the disk continuously sping, and "a controller" must continually endeavor throughout the "seek time":

> "(1) to maintain the head at or very near the track centerline while writing or reading and (2) to move the head rapidly from one track to another so as to minimize the time taken to locate the head at or near the centerline of the target track."[171]

This endeavor is achieved by "regulating movement of said head" and this use of "a controller regulating movement of said head" is performed, at least in part after the completion of "seek time" associated with a corresponding "command from the host computer to search a track and position of the transducer head ... [and thereby] controlling the position of the transducer heads 4",[172] "based on at least one of said first data address mark and said second data address mark"[173] informing "that the data is started ...", thereby ending one iteration of a read operation. The record before the Board therefore demonstrates that both the *written description* clause and the *enablement* clause have been met by Appellant's application.

35 U.S.C. §102(e)

Contrary to the instance of the Examining Staff, there is no anticipation of any of claims 1 through 3, 6, 16, 17, 20, 21, 24, 26 through 28, 31, 32, 35 through 51 and 54 are again rejected

---

171 U.S. Patent № 5.510.939 for *Disk Drive With Adaptive Positioning* to M. M. Lewis, 23rd of April 1996, column 1, lines 37-43.

172 Son '387, column 5, lines 38-46.

173 Claims 32-34 and 50-52.

under 35 U.S.C. §102(e) by Malone Sr. '497. Hornbook law teaches that there can be no anticipation under 35 U.S.C. §102(e) unless all of the elements in a claim are found in exactly the same situation and united in the same way in a single prior art reference, and thus every element must be literally present and must also be arranged as in the claim.[174] Not all elements of these claims are found in Malone '497; by way of example, Malone '497 does not teach Appellant's *data address marks*, and in point of fact, does not use the art recognized term *data address mark*.

To find anticipation, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art."[175] Here, the Examining Staff simply seeks to shoehorn the structurally different *servo address mark* into performing the operational office of Appellant's *data address mark*, despite the art recognized distinctions between these components and despite the functional inability of *servo address mark*, whether singular or plural in number, to serve as a *data address mark* by "inform[-ing] that the data is started"[176] or to provide the "necessary synchronization when data is recorded or read from the magnetic disk."[177] In simpler terms, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."[178] As is explained by

---

174 *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (CAFC 1989).

175 *In re Wilson*, 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970), and the Manual of Patent Examining Procedure, 8th Edition, Rev. 5, §2143.03.

176 Son '387, column 2, line 65.

177 Son '387, column 2, lines 66 and 67.

178 *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Malone '830,

> "[a] data track for any of the preceding formats typically comprises 'splices' of data. That is, portions of data will be written to the track at different times, and consequently, the frequency of each portion will not be synchronous with other portions of the same track."[179]

Recognizing the absence of structural anticipation, the absence of functional anticipation, and the absence of anticipation of Appellant's results, there is no anticipation of claims 1 through 3, 6, 16, 17, 20, 21, 24, 26 through 28, 31, 32, 35 through 51 and 54 under 35 U.S.C. §102(e) by Malone Sr. '497.[180]

Returning again to Appellant's metaphor, a motorist proceeding along a single lane of highway will encounter both a *stop bar* and a *stop light* in close proximity to one another. Their functions are related, but are not interchangeable.[181] Both a *sync address mark* and a *data address mark* will be encountered by a head as it travels along a track on the disk; only the *data address mark*, as opposed to a *sync address mark*, "informs that the data is started" (*i.e.*, that the signal which is being currently detected is user data). In summary, Malone '497 neither teaches

---

179 Daniel James Malone, Sr., U.S. Patent 6.392.830 B1 issued on the 21st of May 2002, entitled *System And Method For Providing Nonadjacent Redundancy Synchronization Bytes*,column 2, lines 20-24.

180 Malone '830 is a divisional of Serial No. 08/782.207 filed on 10th January 1997, and issued as U.S. Patent No. 6.124.994, which is a divisional of Serial No. 08/570.878 filed on 12th December 1995, and issued as U.S. Patent No. 6.181.497 (*i.e.*, Malone '497).

181 By statute, a *stop light* (or a *stop sign*) instructs a motorist *when* to stop and only a *stop bar* instructs the motorist about the precise and exact location *where* that stop, which is being required by the *stop light*, must be completed. In the same sense, it is only a *data address mark*, rather than a *sync address mark*, which "informs that the data is started" (*i.e.*, that the signal which is being currently detected is user data).

nor suggests either the structure, function or location of *data address marks* – Malone '497 simply does not mention *data address marks*.[182] Consequently, there is no anticipation under 35 U.S.C. §102(e).

Current U.S. practice demands that "there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention."[183] Where, as here, there are art recognized structural and functional differences, as well as differences in the results of the seek reliability attained, that are both recognized in the art and identified by the inventor of Malone '497, and the existence of none of these differences are in dispute in the record before the Board, there is no anticipation. A refusal to sustain these rejections is respectfully urged.

35 U.S.C. §103(a)

Examiner's proposed combination would incorporate the two "sync byte fields 14, 62" and employ those synch byte fields for the same purpose, and with the same results as are taught by Malone '497, without consideration of either the structural inability of a disk drive as defined by claims 11 through 15, or a method for forming and processing a data sector as defined by

---

182 The Examining staff seeks to dwell on superficial similarities and accidents of nomenclature between *sync address marks* and *data address marks*. By metaphor, both a *stop light* and a *stop bar* are physically placed in proximity as traffic control devices. State motor vehicle codes define *stop lights* and a *stop bars*, and on a superficial sense, both are in close proximity to one another and both direct a motorist where to stop a motor vehicle.

183 *Scripps Clinic & Research Foundation v. Genentech, Inc.*, 927 F.2d 1565, 18 USPQ2d 101, 18 USPQ2d 186 (Fed. Cir. 1991).

claims 7 through 10, could be reliably employed within the extremely short interval of "seek time" allotted, to "inform that the data is started and provide necessary synchronization when the magnetic disk driving apparatus reads the data."[184] Although the record before the Board is silent upon both justification for making the modification of the art advocated by the Examining Staff, as well as the existence of motivation for the combination, the sole basis appears to be a confusion by the Examining Staff which is attributable to an accidental similarity in the art to given names of the *servo address marks* and the *data address marks*. No explanation is given by the Examining Staff.

Moreover, the advantage attainable with the practice of claims 7 and 11 is unavailable with the Examiner's proposed modification of the primary reference simply because incorporation of the two "sync byte fields 14, 62" taught by Malone '497 and employment of those synch byte fields necessarily restricts the combination of the Examining Staff to the same results as are taught by Malone '497, simply because, for among other deficiencies, the two "sync byte fields 14, 62" taught by Malone '497 physically can not serve to "informs that the data is started and provides the necessary synchronization"[185] as is required by Appellant's structure and process because, for among other reasons, no one of ordinary skill in the art is, on the record before the Board, known to have taught that "a servo address mark" is capable of "inform[-ing] that the data is started".[186] In short, neither Appellant's improvement in the resulting seek and

---

184 Son '387, column 4, lines 35-37.

185 Son '387, column 4, lines 35-38.

186 Son '387, column 2, line 65.

read reliability are attained with the Examining Staff's proposed modification, nor are the resulting structural or operational modifications of the art made by Appellant; simply put, two "synch byte fields" are not fungible or interchangeable. A mere accidental similarity in art given names, and a serendipitous coincidence in the number of *synch byte fields* taught by Malone '497 and *data address fields* taught by Appellant is inadequate to make a *prima facie* showing of obviousness. Accordingly, absent either Appellant's structure,[187] operational mode and advantageous results, and absent evidence in the record of either a *prima facie* showing of obviousness,[188] the motivation for modifying the primary reference in the manner required by the Examiner's proposed combination, this rejection of claims 7 through 15 may not be maintained

35 U.S.C. §251

The Examining staff seems to have ignored the guidance kindly provided by the special efforts of the Board of Patent Appeals and Interferences as may be found in, by way of example, the precedential *Ex parte Daniel M. Eggart, et al.*, Appeal № 2001-0790, Serial № 09/110,145, decided on the 29th of May 2003. A copy of that Opinion was previously enclosed by this

187 Malone '497 itself recognizes these structural differences: "As a result there are *phase differences between the two sets of fields*. Hence, the preamble 32 and synch char 34 are used for reading the header 28A, and the preamble 40 and synch char 42 are used to read data 28B." Amendment filed on the 25th of January 1999, pages 2 through 4, during prosecution of Malone '497, Patent № 6.181.497, Serial № 08/570.878.

188 35 U.S.C. §103(a) mandates consideration of "*the differences* between the subject matter sought to be patented and the prior art ... ." Substitution of obliviousness of the Examining Staff to "*the differences*" for the statutorily mandated consideration does not produce a *prima facie* showing of obvious; "*the differences*" must firstly be identified by the Examining Staff and must secondly, be weighted in the light of a person of ordinary skill in the art. Anything less fails the statutory showing of obviousness required by 35 U.S.C. §103(a) before a claim may be rejected.

Appellant for the Examiner's guidance. As explained in that Opinion, when the Appellant's claim 1 was "met by a final rejection", the Appellant had two options: "appeal the Examiner's final rejection" or "amend that claim in an attempt to define narrower, patentable subject matter." The Appellant in that Opinion "chose the latter option and amended claim 1 a second time" and, "upon consideration of claim 1 (twice amended), the Examiner determined that that was patentable." As further explained by the Board,

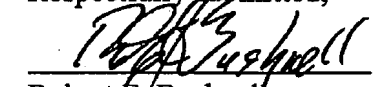
> "due to the vagaries of using words to describe a mechanical object ... it is not unreasonable to conclude that errors can be made in choosing the most correct language to define the mechanical object in a way which is consistent with the invention described in the patent application and is patentable over the prior art."

Thus, "a patentee who believes he has claimed less than he has a right to claim in the patent through error without any deceptive intent may file an application for a reissue application." In the *Eggart* Opinion, the Board explained that the Appellant had never conceded that the broader scope of coverage provided by the reissue claims was unpatentable. Similarly, in the instant application and in the parent application, Appellant has never maintained and has advanced no action to suggest during the prosecution of the parent application that the difference in scope of coverage between the patent's issued claims and reissue claims 16 through 54, was "unpatentable." As explained by the Board, "therefore, in our view, such subject matter is not barred by the recapture rule. In short, the absence of "skipping a remaining data address" and "said transducer head not utilizing a remaining data address mark" in the rejected reissue claims is irrelevant to the question of reissue recapture, where as in the *Eggart* Opinion, Appellant here simply chose to present amended claim 1 in view of the Examiner's earlier indication of the

allowability of dependent claim 2. Consequently, the requisite basis for a reissue recapture under 35 U.S.C. §251 is lacking. Withdrawal of this rejection is therefore respectfully requested.

In view of the law and facts stated herein as well as all the foregoing reasons, Appellant believes that the rejections are improper and respectfully requests that the Board refuse to sustain the outstanding rejections of claims 1 through 54.

Respectfully submitted,



Robert E. Bushnell,
Attorney for the Appellant
Registration No.: 27,774

1522 "K" Street N.W., Suite 300
Washington, D.C. 20005
(202) 408-9040

Folio: P54757RE2
Date: 4/11/07
I.D.: REB/kf

VIII. CLAIMS APPENDIX

Claims 1-54

1. A method for forming and processing a data address mark positioned in a data track of a magnetic disk preceding a data region in a disk drive to establish synchronization requested for reading user data from the magnetic disk, said method comprising the steps of:

recording of said data address mark in at least two different recording locations of said data track;

when one data address mark recorded in said different recording locations of said data track is normally detected to establish synchronization requested for reading user data from the magnetic disk, regarding said one data address mark as an effective data address mark of a corresponding data region; and

skipping a remaining data address mark recorded in said different recording locations of said data track, when any one data address mark recorded in said different recording locations is normally detected.

2. The method of claim 1, said at least two different recording locations corresponding to at least a first location and a separately located second location, said data address mark recorded in said first location being in accordance with a first pattern, and said data address mark recorded in said second location being in accordance with a second pattern different from said first pattern.

3. (Amended) The method of claim 2, further comprised of each [of] said data address mark recorded in said different recording locations of said data track being constructed of one byte of information.

4. (Amended) The method of claim 3, further comprised of bits constructing said one byte being utilized for recording said data address mark and for counting the number of a byte

of said remaining data address mark.

5. The method of claim 4, further comprised of said data address mark being detected by a controller of said disk drive performing a masking function with respect to said data address mark.

6. The method of claim 1, further comprised of said data address mark being detected by a controller of said disk drive performing a masking function with respect to said data address mark.

7. (Amended) A method for forming and processing a data sector comprising an identification field and a data field in a magnetic disk of a headerless servo recording system, comprising the steps of:

recording a data address mark, during a recording mode, in at least two different locations of said data field immediately preceding a data area containing user data;

detecting said data address mark recorded in said different locations of said data field, during a reading mode, to confirm validity of user data contained in said data area following said data address mark;

when said data address mark recorded in at least one of said different locations of said data field is detected, regarding said [one] data address mark <u>detected</u> as an effective data address mark of a corresponding data area for confirming the validity of user data contained therein; and

skipping a remaining data address mark recorded in said different recording locations of said data track, when said data address mark recorded in said at least one of said different recording locations is detected.

8. The method of claim 7, said at least two different locations corresponding to at least a first location and a separately located second location, said data address mark recorded in said

first location being in accordance with a first pattern and said data address mark recorded in said second location being in accordance with a second pattern different from said first pattern.

9. (Amended) The method of claim 7, further comprised of each [of] said data address mark recorded in said different recording locations of said data field being constructed of one byte of information.

10. The method of claim 7, further comprised of said identification field comprising an identification preamble, an identification address mark, an identification area for providing said identification information, a cyclic redundancy code, and an identification postamble.

11. A disk drive, comprising:

a data recording disk having a plurality of concentric tracks, each track having servo sectors in which servo information for use in positioning a transducer head is written and succeeding data sectors, each data sector including:

an identification region in which identification information for use to identify the data sector for reading and writing operations is written; at least two different data address mark regions for use to indicate a validity of data recorded on said data sector is written;

a data region in which data transferred from an external communication device is written; and

an error correction code region in which an error correction code for use to automatically correct an error is written;

said transducer head for writing data to and reading data from the data sectors of the data recording disk, and for reading servo position information from the servo sectors of the data recording disk;

means attached to the transducer head for positioning the head across the tracks to perform said read and write operations; and

said transducer head not utilizing a remaining data address mark recorded in said different recording locations of said data track, when a data address mark recorded in said two different data address regions is detected.

12. The disk drive of claim 11, further comprised of said transducer head detecting data address marks recorded in at least two different data address mark regions of said data field, during said reading mode, to confirm validity of user data contained in said data area following said data address mark, and when at least one data address mark recorded in said two different data address mark regions of said data field is detected, regarding said one data address mark as an effective data address mark of a corresponding data area for confirming the validity of user data contained therein.

13. The disk drive of claim 12, said at least two different data address mark regions of said data field corresponding to at least a first region and a separately located second region, said data address mark recorded in said first region being in accordance with a first pattern and said data address mark recorded in said second region being in accordance with a second pattern different from said first pattern.

14. The disk drive of claim 11, further comprised of each data address mark recorded in said two different data address mark regions of said data field being constructed of one byte of information.

15. The disk drive of claim 11, further comprised of said identification field comprising an identification preamble, an identification address mark, an identification area for providing said identification information, a cyclic redundancy code, and an identification postamble.

16. A method of providing a data block preceding a servo information area in a magnetic recording medium for accessing user data therefrom, comprising:

writing a first data address mark in said data block; and

writing a second data address mark in said data block at a location preceding said servo information area.

17. The method of providing said data block in accordance with claim 16, wherein said step of writing said first data address mark comprises:

writing a first plurality of bits of a first bit pattern; and

wherein said step of writing said second data address mark comprises:

writing a second plurality of bits of a second bit pattern different from said first bit pattern.

18. The method of providing said data block in accordance with claim 17, wherein:

at least one bit of said first plurality of bits represents a first byte count signifying a first number of bytes to be ignored when said first data address mark is normally read.

19. The method of providing said data block in accordance with claim 18, wherein:

at least one bit of said second plurality of bits represents a second byte count signifying a second number of bytes to be ignored when said second data address mark is normally read.

20. A magnetic recording medium having a data track having one or more data blocks preceding a servo information area, comprising:

a first data address mark located before said servo information area in a first data block; and

a second data address mark located before said servo information area in said first data block.

21. The magnetic recording medium according to claim 20, wherein:

said first data address mark comprises a first plurality of bits of a first bit pattern; and

said second data address mark comprises a second plurality of bits of a second bit pattern different from said first bit pattern.

22. The magnetic recording medium according to claim 21, further comprised of:

at least one bit of said first plurality of bits being a first byte count signifying a first number of bytes to be ignored when said first data address mark is normally read.

23. The magnetic recording medium in accordance with claim 22, wherein:

at least one bit of said second plurality of bits represents a second byte count signifying a second number of bytes to be ignored when said second data address mark is normally read.

24. A disk drive device, comprising:

a magnetic recording medium having at least one data block that includes at least a first data address mark and a second data address mark having no servo information area therebetween; and

a controller configured to read within said at least one data block at least one of said first data address mark and said second data address mark.

25. The disk drive device according to claim 24, wherein:

said controller is further configured to read a predetermined number of bits from a successfully read one of said at least first data address mark and said second data address mark, and to determine a number of bytes to be ignored based on said predetermined number of bits.

26. A method for reading a data block preceding a servo information area of a memory disk, said method comprising the steps of reading at least one of a plurality of data address marks recorded on said data block at a location before said servo information area.

27. The method of claim 26, further comprised of skipping detection of other ones of said

at least two data address marks from subsequent ones of said different recording locations.

28. The method of claim 26, wherein recording of said at least two data address marks comprises:

recording a first data address mark at a first one of said plurality of different locations, said first data address mark comprising a first plurality of bits of a first bit pattern; and

recording a second data address mark at a second one of said plurality of different locations, said second data address mark comprising a second plurality of bits of a second bit pattern from said first bit pattern.

29. The method of claim 28, wherein:

at least one bit of said first plurality of bits being a first byte count signifying a number of bytes to be ignored when said first data address mark is normally read at said first one of said plurality of different locations.

30. The method of providing said data block in accordance with claim 29, wherein:

at least one bit of said second plurality of bits represents a second byte count signifying a second number of bytes to be ignored when said second data address mark is normally read.

31. A method for preparing a memory disk, comprising:

recording a data address mark providing synchronization that enables reading of data from the memory disk, along a data track on the memory disk at a first location on a first data block preceding a servo information area; and

recording said data address mark at a second location on said first data block preceding said servo information area.

32. A disk drive device, comprising:

a head positioned to read, within at least one of a plurality of data blocks of a recording

medium, a first data address mark, and a second data address mark, said first data address mark and said second data address mark having no servo information therebetween; and

a controller regulating movement of said head based on at least one of said first data address mark and said second data address mark.

33. The device of claim 32, wherein:

said head reading within said first data address mark, an indication of a number of bytes to be ignored within said data block subsequent to successfully reading of said first data address mark.

34. The device of claim 32, wherein:

said controller is further configured to read a predetermined number of bits from a successfully read one of said first data address mark and said second data address mark, and to determine a number of bytes to be ignored based on said predetermined number of bits.

35. A method of providing a data block preceding a servo information area in a magnetic recording medium for accessing user data therefrom, comprising:

writing a first data address mark in said data block; and

writing in said data block at a location preceding said servo information area, a second data address mark that is distinguishable from said first data address mark.

36. A method of providing a data block preceding a servo information area in a magnetic recording medium for accessing user data therefrom, comprising:

writing a first data address mark in said data block; and

writing a second data address mark exhibiting a different bit pattern in said data block at a location preceding said servo information area.

37. A method of providing a data block preceding a servo information area in a magnetic

recording medium for accessing user data therefrom, comprising:

writing in said data block a first data address mark marking said data block; and

writing in said data block at a location preceding said servo information area, a second data address mark separately marking said data block.

38. A magnetic recording medium having a data track having one or more data blocks preceding a servo information area, comprising:

a first data address mark located before said servo information area in a first data block; and

a second data address mark distinguishable from said first data address mark, located before said servo information area in said first data block.

39. A magnetic recording medium having a data track having one or more data blocks preceding a servo information area, comprising:

a first data address mark located before said servo information area in a first data block; and

a second data address mark exhibiting a different bit pattern, located before said servo information area in said first data block.

40. A magnetic recording medium having a data track having one or more data blocks preceding a servo information area, comprising:

a first data address mark located before said servo information area in a first data block; and

a second data address mark separately marking said data block, located before said servo information area in said first data block.

41. A disk drive device, comprising:

a magnetic recording medium having at least one data block that includes at least a first

data address mark and a second data address mark distinguishable from said first data address mark and having no servo information area between said first data address mark and said second data address mark; and

a controller configured to distinguish within said at least one data block, between said first data address mark and said second data address mark.

42. A disk drive device, comprising:

a magnetic recording medium having at least one data block that includes at least a first data address mark and a second data address mark exhibiting a different bit pattern, with no servo information area between said first data address mark and said second data address mark; and

a controller configured to read within said at least one data block at least one of said first data address mark and said second data address mark.

43. A disk drive device, comprising:

a magnetic recording medium having at least one data block that includes at least a first data address mark and a second data address mark separately marking said data block, with no servo information area between said first data address mark and said second data address mark; and

a controller configured to read within said at least one data block at least one of said first data address mark and said second data address mark.

44. A method for reading a data block preceding a servo information area of a memory disk, said method comprising the steps of reading at least one of a plurality of data address marks that are mutually distinguishably on the memory disk at a location before said servo information area.

45. A method for reading a data block preceding a servo information area of a memory

disk, said method comprising the steps of reading at least one of a plurality of data address marks exhibiting different bit patterns on the memory disk at a location before said servo information area.

46. A method for reading a data block preceding a servo information area of a memory disk, said method comprising the steps of reading at least one of a plurality of data address marks that separately mark said data block on the memory disk at a location before said servo information area.

47. A method for preparing a memory disk, comprising:

recording a first data address mark providing synchronization that enables reading of data from the memory disk, along a data track on the memory disk at a first location on a first data block preceding a servo information area; and

recording a second data address mark that is distinguishable from said first data address mark at a second location on said first data block preceding said servo information area.

48. A method for preparing a memory disk, comprising:

recording a first data address mark providing synchronization that enables reading of data from the memory disk, along a data track on the memory disk at a first location on a first data block preceding a servo information area; and

recording a second data address mark exhibiting a different bit pattern, at a second location on said first data block preceding said servo information area.

49. A method for preparing a memory disk, comprising:

recording a data address mark providing synchronization that enables reading of data from the memory disk, along a data track on the memory disk at a first location on a first data block preceding a servo information area; and

recording said data address mark to separately mark said data block at a second location

on said first data block preceding said servo information area.

50. A disk drive device, comprising:

a head positioned to read, within at least one data block of a recording medium, a first data address mark, and a second data address mark that is distinguishable from said first data address mark; and

a controller regulating movement of said head based on at least one of said first data address mark and said second data address mark.

51. A disk drive device, comprising:

a head positioned to read, within at least one data block of a recording medium, a first data address mark, and a second data address mark separately marking said data block; and

a controller regulating movement of said head based on at least one of said first data address mark and said second data address mark.

52. A disk drive device, comprising:

a head positioned to read, within at least one data block written in headerless servo recording format on a recording medium, a first data address mark, and a second data address mark separately marking said data block; and

a controller regulating movement of said head based on at least one of said first data address mark and said second data address mark.

53. A method of providing a data block recording medium for accessing user data therefrom, comprising:

writing within at least one data block written in a headerless servo recording format on said recording medium, a first data address mark marking said data block; and

writing in said data block, a second data address mark separately marking said data block.

54. A method of providing a data block in a recording medium for accessing user data therefrom, comprising:

writing in said data block a first data address mark marking said data block; and

writing in said data block a second data address mark separately marking said data block.

IX. EVIDENCE APPENDIX

1. U.S. Patent № 4,618,989 to Young, *et al.*, issued on 21 October 1986.[189]
2. U.S. Patent № 5,047,877 to Herting, Kenneth E., issued on 10 September 1991.[190]
3. U.S. Patent № 5,210,660 to Hetzler, Steven R., issued on 11 May 1993.[191]
4. U.S. Patent № 5,231,545 to Gold, Clifford M. issued on 27 July 1993.[192]
5. U.S. Patent № 5,347,207 to Otsuki, Tadashi issued on 13 September 1994.[193]
6. U.S. Patent № 5,379,160 to Otani, Kazuoki, issued on 3 January 1995.[194]
7. U.S. Patent № 5,384,671 to Fisher, Kevin D. issued on 24 January 1995.[195]
8. U.S. Patent № 5,420,730 to Moon, *et al.*, issued on 30 May 1995.[196]
9. U.S. Patent № 5,438,559 to Best, *et al.*, issued on 1 August 1995.[197]
10. U.S. Patent № 5,442,499 to Emori, Teruaki issued on 15 August 1995.[198]
11. U.S. Patent № 5,446,604 to Chiba, Takayoshi, issued on 29 August 1995.[199]
12. U.S. Patent № 5,475,540 to Gold, Clifford M., issued on 12 December 1995.[200]

---

189 Cited in the first Office action (Paper № 5) dated 5/30/2002.

190 Cited in the fourth Office action (Paper № 20050510) dated 5/18/2005.

191 Cited in the first Office action (Paper № 5) dated 5/30/2002.

192 Cited in the first Office action (Paper № 5) dated 5/30/2002.

193 Cited in the first Office action (Paper № 5) dated 5/30/2002.

194 Cited in the fourth Office action (Paper № 20050510) dated 5/18/2005.

195 Cited in the first Office action (Paper № 5) dated 5/30/2002.

196 Cited in the first Office action (Paper № 5) dated 5/30/2002.

197 Cited in the first Office action (Paper № 5) dated 5/30/2002.

198 Cited in the first Office action (Paper № 5) dated 5/30/2002.

199 Cited in the fourth Office action (Paper № 20050510) dated 5/18/2005.

200 Cited in the first Office action (Paper № 5) dated 5/30/2002.

13. U.S. Patent № 5,517,631 to Machado, *et al.*, issued on 14 May 1996.[201]
14. U.S. Patent № 5,523,903 to Hetzler, *et al.*, issued on 4 June 1996.[202]
15. U.S. Patent № 5,544,135 to Akin, *et al.*, issued on 6 August 1996.[203]
16. U.S. Patent No.5,581,418 to Hasebe, Masahiro, issued on 3 December 1996.[204]
17. U.S. Patent № 5,477,103 to Romano, *et al.*, issued on 19 December 1996.[205]
18. U.S. Patent № 5,589,998 to Yu, Mantle M., issued on 31 December 1196.[206]
19. U.S. Patent № 5,627,693 to Hirukawa, Takashi, issued on 6 May 1997.[207]
20. U.S. Patent № 5,627,695 to Prins, *et al.*, issued on 6 May 1997.[208]
21. U.S. Patent № 5,631,783 to Park, Jung-il, issued on 20May 1997.[209]
22. U.S. Patent № 5,696,745 to Yamawaki, Masashi, issued on 9 December 1997.[210]
23. U.S. Patent № 5,742,582 to Suzuki, Katsuji, issued on 21 April 1998.[211]
24. U.S. Patent № 5,825,569 to Kim, *et al.*, issued on 20 October 1998.[212]

---

201 Cited in the first Office action (Paper № 5) dated 5/30/2002.

202 Cited in the first Office action (Paper № 5) dated 5/30/2002.

203 Cited in the first Office action (Paper № 5) dated 5/30/2002.

204 Cited in the first Office action (Paper № 5) dated 5/30/2002.

205 Cited in the first Office action (Paper № 5) dated 5/30/2002.

206 Cited in the first Office action (Paper № 5) dated 5/30/2002.

207 Cited in the first Office action (Paper № 5) dated 5/30/2002.

208 Cited in the first Office action (Paper № 5) dated 5/30/2002.

209 Cited in the first Office action (Paper № 5) dated 5/30/2002.

210 Cited in the first Office action (Paper № 5) dated 5/30/2002.

211 Cited in the first Office action (Paper № 5) dated 5/30/2002.

212 Cited in the first Office action (Paper № 5) dated 5/30/2002.

25. U.S. Patent № 5,844,920 to Zook, *et al.*, issued on 1 December 1998.[213]

26. U.S. Patent № 6,181,497 to Malone, Sr., Daniel James, issued on 30 January 2001.[214]

---

213 Cited in the fourth Office action (Paper № 20050510) dated 5/18/2005.

214 Cited in the fourth Office action (Paper № 20050510) dated 5/18/2005.

X. RELATED PROCEEDINGS APPENDIX

None.